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MODEL 739

PRINTER

37400910 REV B

FEBRUARY 1982

TECHNICAL MANUAL

TP 7-80

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4/80 Rev. B

MODEL 739

PRINTER

37400910 REV B FEBRUARY 1982

TECHNICAL MANUAL

REVISION ADDENDUM

MODEL 739 TECHNICAL MANUAL

The following Publication Change Pages (PCPs) constitute a revision to the current manual due to changes and improvements in the printer.

The addendum consists of the following PCPs and affects the following assemblies:

PCN/PCP	Number	Affected Assembly Title

---- Refer to the next 3 pages.----

The addition of this revision addendum updates the Model 739 Printer Technical Manual from July 1981, Rev. A to February 1982, Rev. B.

PUBLICATION CHANGE PAGES

PCP NO. 37400910/A.A ☐ CLERICAL CHANGE ☒ DESIGN CHANGE DATE 24 NOV 81

PUBLICATION AFFECTED	REV	PCP SEQ. NO.	ASSEMBLY AFFECTED NUMBER	OLD REV.	NEW REV.	ECO
739 Technical Manual	A	A	63680192	A2	A3	1295

These pages supplement information provided by the following Equipment Change Bulletins.

These PCP sheets reflect changes to the equipment that have not yet been documented in the technical publications or are simply clerical corrections to the specific pages in the manual. For documentation on your unit, always replace/delete/add the pages as noted below and verify the changes are applicable to your particular printer.

PUBLICATION ACTIONS

REPLACEMENT PAGES		DELETE PAGES		ADD PAGES	
6-2	6-4				
6-5	6-6				

COMMENTS

PURPOSE: This PCP describes a minor change to the 63680192 Logic PCB.

Two 0.1 uF capacitors have been added; one in the ONLINE/LOCAL select circuit and one in the Line-Feed stepping motor circuit. The purpose of the capacitors is to improve noise immunity.

DIRECTIONS: Replace pages 6-2, 6-4, 6-5 and 6-6, or draw in the two capacitors as illustrated.

NOTE:
Some users may have printers which are accurately documented by the contents of the current manual prior to this PCP.
These users should retain the pages noted with an asterisk (*) and add these pages as a supplement for future reference.

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PUBLICATION CHANGE PAGES

PCP NO. 37400910/A.B ☐ CLERICAL CHANGE ☒ DESIGN CHANGE DATE 26 JAN '82

PUBLICATION AFFECTED	REV	PCP SEQ. NO.	ASSEMBLY AFFECTED			
			NUMBER	OLD REV.	NEW REV.	ECO
739 Technical Manual P/N 37400910	A	B	63680192-4001	A8	A9	001356

These pages supplement information provided by the following Equipment Change Bulletins.

These PCP sheets reflect changes to the equipment that have not yet been documented in the technical publications or are simply clerical corrections to the specific pages in the manual. For documentation on your unit, always replace/delete/add the pages as noted below and verify the changes are applicable to your particular printer.

PUBLICATION ACTIONS

REPLACEMENT PAGES		DELETE PAGES		ADD PAGES	

COMMENTS

PURPOSE: This PCP describes a minor change to the Logic PCB (63680192-4001) that involves adding two capacitors (C51, C52; .022uF) and replaces one capacitor (C48 removed, replaced by C53; 0.33uF). This change (ECO 001356) reduces RFI (Radio Frequency Interference) caused by the printer. This does not change the function of the printer in any way.

DIRECTIONS: Refer to page 2 of this PCP for illustrations of the addition of the 3 capacitors.

NOTE:
Some users may have printers which are accurately documented by the contents of the current manual prior to this PCP.
These users should retain the pages noted with an asterisk (*) and add these pages as a supplement for future reference.

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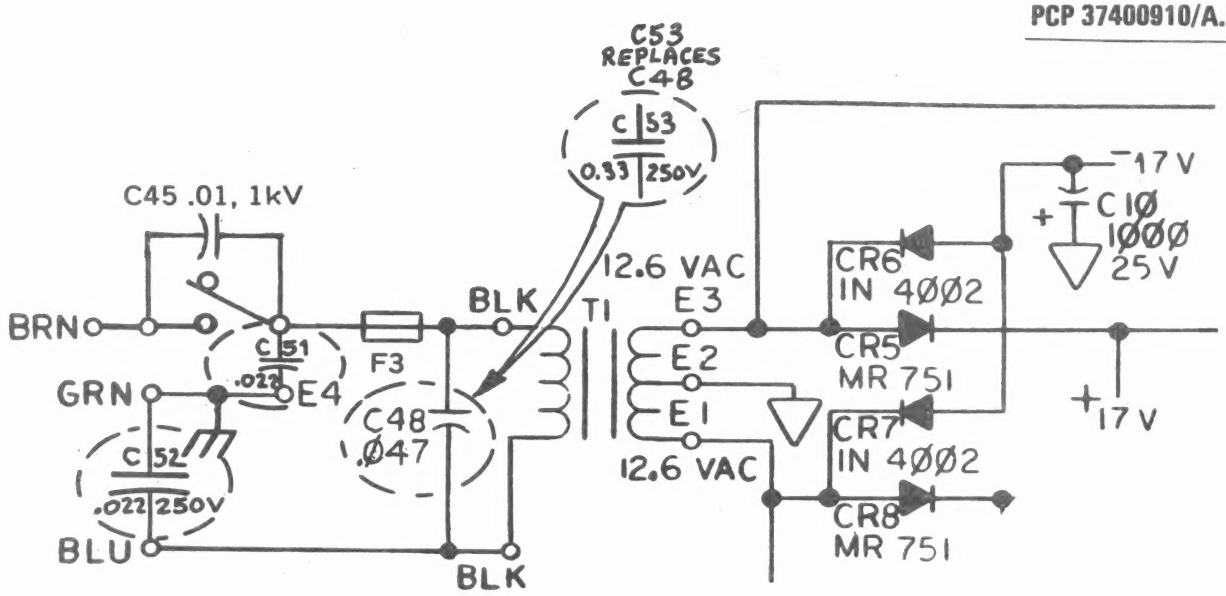

Figure 1 C51, C52, C53 shown on print 63680193

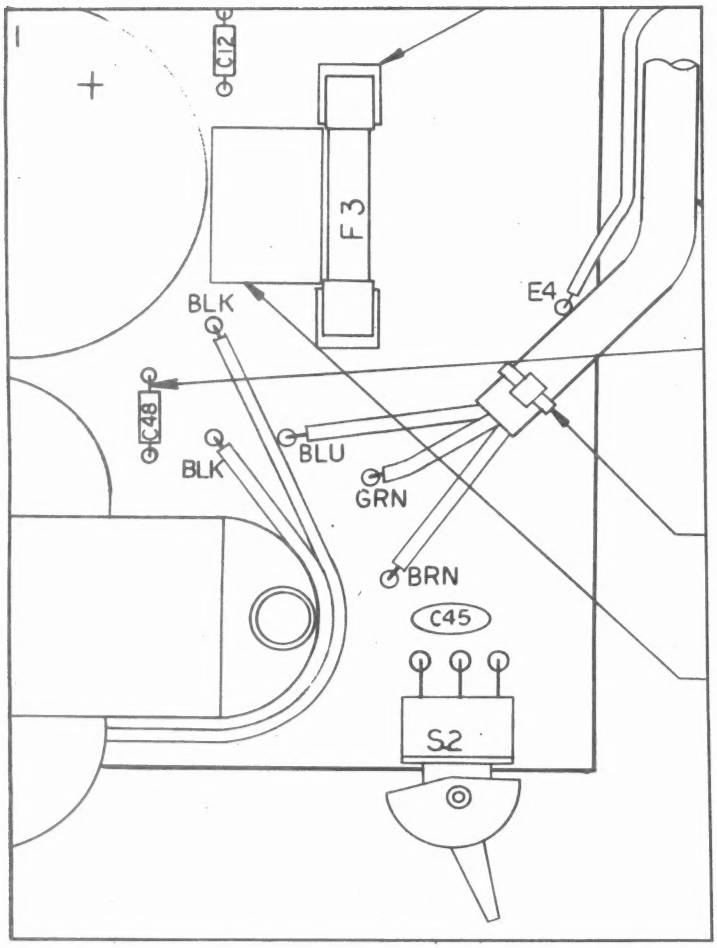

Figure 2 Before ECO 001356 (Rev. A8)

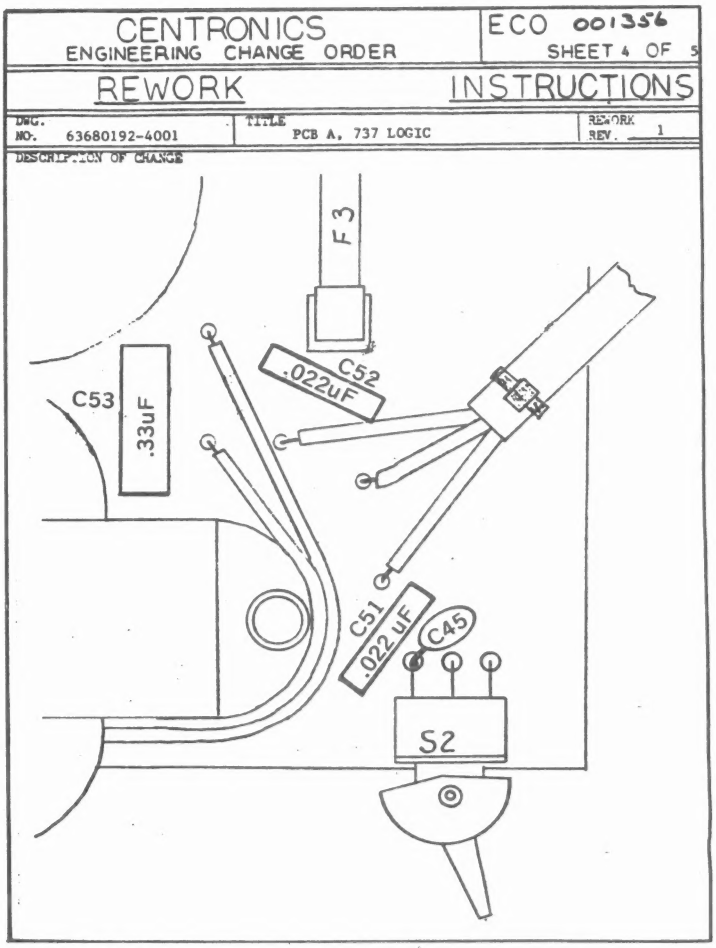

Figure 3 After ECO 001356 (Rev. A9)

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SECTION 1
GENERAL INFORMATION

1.1 SCOPE OF THIS MANUAL

This manual contains detailed information on the theory, maintenance, adjustment and parts replacement of the Centronics Model 739 dot matrix printers. The differences between the models are outlined in paragraph 1.2. The contents of this manual are intended for use by qualified service personnel who are trained in the maintenance of electronic and electro-mechanical equipment. Operation, installation, preventive maintenance, character set samples, control codes and interface information are covered in the Operators Manual P/N 37400911-9001.

1.2 DESCRIPTIONS OF 739 MODELS

(739-1) - Parallel input; 120 VAC, 60 Hz; 228 mm pinfeed roller.

(739-2) - Parallel input; 230 VAC, 50 Hz; 228 mm pinfeed roller (739-2L has 238 mm pinfeed roller, VDE compliance).

(739-3) - Serial RS232C input; 120 VAC, 60 Hz; 228 mm pinfeed roller; 512 byte buffer (739-3B has 2K buffer).

(739-4) - Serial RS232C input; 230 VAC, 50 Hz; 228 mm pin feed roller (739-4L has 238 mm pinfeed roller); 512 byte buffer (739-4B has 2K buffer); all 739-4 models, VDE compliance.

(739-5) - Serial 20 mA current loop; 120 VAC, 60 Hz; 228 mm pinfeed roller (739-5L has 238 mm pinfeed roller); 512 byte buffer (739-5B has 2K buffer).

(739-6) - Serial 20 mA current loop; 240 VAC, 50 Hz; 228 mm pinfeed roller (739-6L has 238 mm pinfeed roller); 512 byte buffer (739-6B has 2K buffer); all 739-6 models, VDE compliance.

1.3 GENERAL DESCRIPTION

Refer to Figure 1-1. The Model 739 is a compact, parallel-input printer that prints proportionally-spaced and monospaced characters (upper and lower case) in a high-density dot matrix. The proportional character set is printed in an Nx9 (N=6 to 18) dot matrix at an average of 14 characters per inch (cpi). The 10 cpi monospaced characters are formed in a 7x8 dot matrix, 80 characters per 8-inch line. The condensed (16.7 cpi) monospaced character set provides 132 characters per 8-inch line.

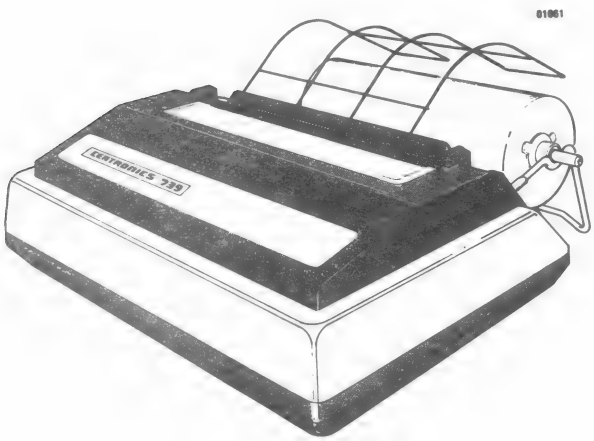
The input code format for the parallel units is 7-bit parallel ASCII, positive true logic. Serial units receive codes at a factory-set baud rate of 9600. Switch pack settings allow baud rate of 50 to 19,200. Using host-generated control codes, the proportional, 10 cpi monospaced and 16.7 cpi monospaced characters can be elongated to form double-width characters; thus, six different styles are available. Right justification of proportional and 16.7 cpi

monospaced characters is accomplished by host-generated justification spaces (dot spaces) of 1 to 6 dot widths. Backspacing and underlining are additional host-controlled functions. Pin-addressable graphics are accomplished using the top six pins. Line feeds for graphics are one-half normal value.

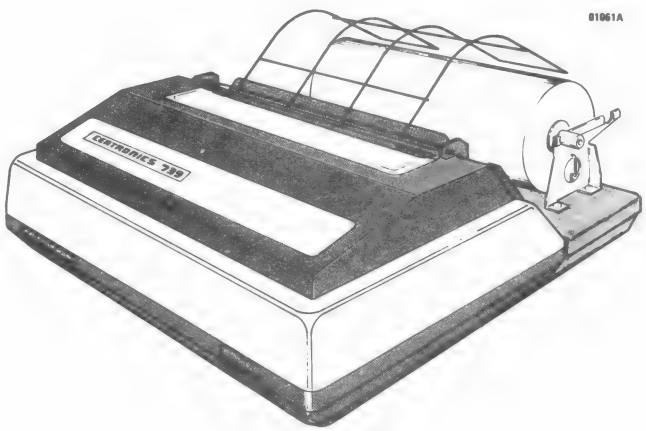
In the ON-LINE mode of operation, control codes provide full and half-line paper feed (forward and reverse) to print subscript and superscript characters. In the LOCAL mode, a front panel switch provides one-line feed or continuous paper feed, forward and reverse.

The paper supply may be standard 9-1/2 inch fanfold forms, 8-1/2 inch roll paper or single sheets. The ribbon is a 15-yard Zip-Pack unit that is easy to replace. The mobius loop in the ribbon insures maximum life, allowing the top and bottom of the ribbon to be used.

The 739 features character sets for six countries: The United States of America, France, United Kingdom, Germany, Italy and Sweden/Finland. The character set is selected by a switch pack setting prior to power-up of the printer. When the power is turned on, the printer logic recognizes the switch settings and is prepared to print characters for that country. Additional country character sets are available as field-installed character ROM's. Refer to the Operators Manual for the description of the character sets for this printer.



739-1, 739-2 Printers



739 Extended Base Printers

Figure 1-1. 739 PRINTERS WITH ROLL PAPER

1.4 SPECIFICATIONS (739-1, 739-2)

Printing Speed	100 characters/second (monospaced); 80 cps (proportional); 371 dots/second (graphics)
Characters Per Line	80 maximum (10 cpi); 132 maximum (16.7 cpi).
Print Width	8 inches (204 mm) maximum.

1.4 SPECIFICATIONS (739-1, 739-2) (continued)

Character Structure	7x8 Dot Matrix (Monospaced) Nx9 Dot Matrix (Proportionally Spaced)
Graphics	6 dots high, 594 dot positions per line (8 inches).
Line Feed Buffer	Capacity for 255 pending line feeds.
Line Feed Repeat Rate	12 line feeds/second.
Vertical Spacing	6 lines per inch (normal line feed).
Horizontal Spacing	Monospaced: 10 or 16.7 characters per inch (cpi). Proportional: 8.2 to 24.6 cpi depending on text; 13 to 14.5 cpi average density. Numerics are monospaced at 12.5 cpi for tabulation.
Parallel Data Input Connector	40-pin PC edge connector.
Code Structure	Standard US ASCII; 7 bits, parallel.
Input Data Rate	Up to 2,200 characters/second.
Character Sets*	Primary: 96 US ASCII monospaced characters. Secondary: 96 US ASCII proportionally-spaced characters.
Input Voltage/Frequency	(739-1) 120 Vac +5%, -10%; 60 Hz $\pm$1 Hz. (739-2) 230 Vac +10%, -5%; 50 Hz $\pm$1 Hz.
Power Requirements	100 watts, maximum.
Size	14-1/2"W x 11"D x 5"H; (368 mm) x (279 mm) x (127 mm)
Weight	12 lbs. (5.4 Kg).
Ribbon (12 per box)	15 Yard Zip-Pack mobius loop (Centronics Part No. 63701712-6001)
Paper Handling	Cut sheets, 8 1/2" (21.6 mm) wide Rolls 3 1/2" to 8 1/2" (88.9 to 21.6 mm) W x 5" (127 mm) diameter, 1" (25.4 mm) core; 3 ply maximum. Fanfold 228 mm (9") pin to pin; adjustable $\pm$1 mm.

*The 739 has switch-selectable country character sets for USA, France, United Kingdom, Germany, Italy and Sweden/Finland (Character Set A).

1.5 SPECIFICATIONS (739-2L)

The specifications for the 739-2L are identical to those of the 739-2 except that the 739-2L has the longer (238 mm) pin feed roller and is configured for VDE compliance. Refer to paragraph 1.4 for all specifications other than listed below. The Operators Manual P/N 37400911 contains all interface information.

Size	14 1/2"W x 16"D x 5 3/4"H (368 mm x 406 mm x 146 mm)
Weight	16 lb. (7.2 kg)
Input Connector	36-pin female

1.6 SPECIFICATIONS (739-3, 739-4)

The specifications for the serial RS232C printers (739-3, 739-4) are listed below. Refer to paragraph 1.4 for other specifications not listed. The Operators Manual P/N 37400911 contains all interface information.

Baud Rate	50 to 19,200 baud (factory set at 9600 baud)
Input Buffer (739-3, 739-4)	512 bytes; 384 bytes indicates buffer full 256 bytes indicates buffer empty
Input Buffer (739-3B, 739-4B)	2048 bytes; 1792 bytes indicates buffer full 256 bytes indicates buffer empty
Input Connector	25-pin EIA female (DB25, RS232C)
Input Data Format:	Start bit, 7 data bits, parity bit, 1 or 2 stop bits
RS232C Levels	Mark=True=Logic 1=-3V to -25V Space=False=Logic 0 = +3V to +25V
Input Voltage/Frequency (739-3)	120 VAC nominal, +5% -10%; 60 Hz $\pm$1 Hz
Input Voltage/Frequency (739-4)	230 VAC nominal +10% -5%; 50 Hz $\pm$1 Hz
Size	14 1/2"W x 16"D x 5.75" H (368 mm x 406 mm x 146 mm)
Weight	16 lb. (7.2 kg)

*7 or 8 data bits, switch selectable; parity even/odd or no parity, switch selectable.

1.7 SPECIFICATIONS (739-5, 739-6)

The specifications for the 20 milliamp current loop printers (739-5, 739-6) are listed below. Refer to paragraph 1.4 for other specifications. The Operators Manual P/N 37400911 contains all interface information.

Baud Rate	50 to 19,200 baud (factory set at 9600 baud)
Input Buffer (739-5, 739-6)	512 bytes; 384 bytes indicates buffer full; 256 bytes indicates buffer empty.
Input Buffer (739-5B, 739-6B)	2048 bytes; 1792 bytes indicates buffer full; 256 bytes indicates buffer empty.
Input Connector	25-pin EIA female (DB25)
Input Data Format*	Start bit, 7 data bits, parity bit, 1 or 2 stop bits.
Current Loop Levels	Mark = True = Logic 1 = 20 mA. Space = False = Logic 0 = 0 mA.
Input Voltage/Frequency (739-5)	120 VAC nominal, +5% -10%; 60 Hz $\pm$1 Hz.
Input Voltage/Frequency (739-6)	230 VAC nominal, +10% -5%; 50 Hz $\pm$1 Hz.
Size	14 1/2"W x 16" D x 5.75" H (368 mm x 406 mm x 146 mm)
Weight	16 lb. (7.2 kg)

*7 or 8 data bits, switch selectable; parity even/odd or no parity, switch selectable.

SECTION 2

THEORY OF OPERATION

2.1 BASIC DESCRIPTION

2.1.1 SERIAL PRINTERS (739-3, 739-4, 729-5, 739-6)

Refer to Figure 2-1. The printer receives ASCII Serial Data from the Data Set through the Interface Cable. The rate of data transmission is determined by the baud (bits per second) rate. The printer's Serial PCB contains baud rate selection switches which are set to agree with the rate of transmission from the host. Data Terminal Ready informs the Data Set that the printer is prepared to receive the data. Data Carrier Detector and Data Set Ready are sent to the interface logic before the Serial Data to guarantee that data sent is valid. The Serial PCB converts the high-level Serial Data to TTL levels which are more suitable to the printer logic circuits. The Serial Data is converted to parallel ASCII codes and stored in RAM (Random Access Memory) until the Logic Board is prepared to receive data. Reverse Channel signals the Data Set that the Input Buffer is temporarily full. Also, Transmit Data sends DC3 (X-OFF) at buffer full (1792 codes for a 2K buffer; 384 codes for 512 buffer) and DC1 (X-ON) when there are 256 codes in the buffer. The main Logic Board requests data by enabling the Demand line. The 8-Bit Data (parallel) is transferred to the logic board by Data Strobe. The data is decoded and printable characters are stored in a print buffer (Memory). When a CR (Carriage Return) or other line-ending code is received, the line is printed. Also, if the print buffer becomes full, the line is automatically printed. Buffer full for the printer is 80 characters (10 cpi), 132 characters (16.7 cpi), or 1186 dot positions (proportional). The Demand line is disabled while printing is being performed. The power supply +5V regulated for the logic, +12V regulated for motor drive, +17V for solenoid and motor drive, and 24 VAC for the ribbon motor. Also, +5V and +17V are supplied to the serial PCB. -17V is supplied to RS232C interface only.

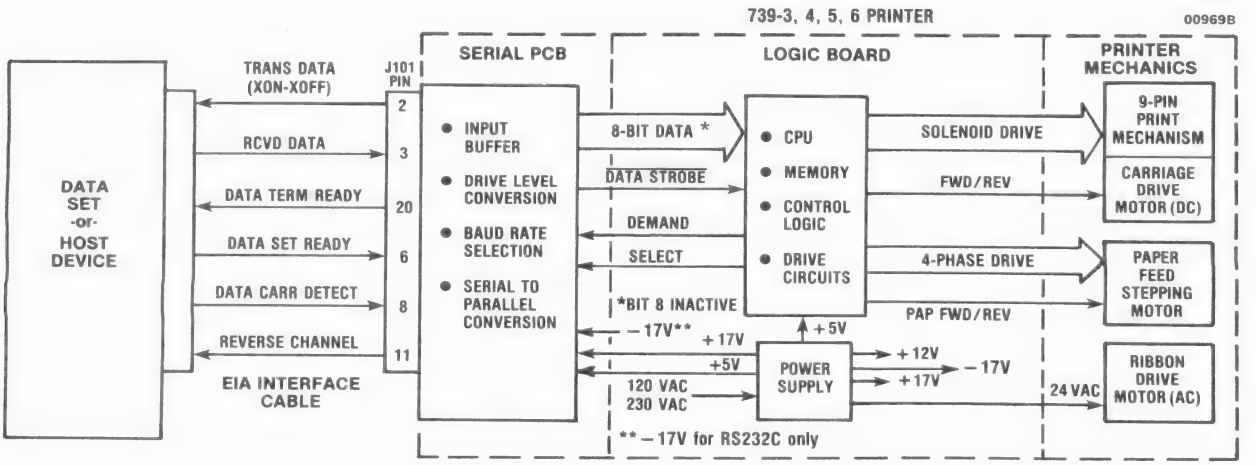


Figure 2-1. 739 SERIAL BLOCK DIAGRAM

2.1.2 PARALLEL PRINTERS (739-1, 739-2)

The printer logic initiates and controls all transmissions from the host device by the control signals SELECT, DEMAND, ACKNLG and BUSY. The host device transmits 8-bit parallel ASCII data and a strobe (8th bit inactive) to the printer logic. The data is decoded, processed and/or stored in a print buffer. When the microprocessor has processed a complete line (or when a print command code is sent), the microprocessor directs the printer to print the characters.

The power supply provides +5V regulated for the logic, +5V EXT for host device sense, +12V regulated for motor drive, +17V unregulated for solenoid and motor drive, and 24 VAC for the ribbon motor. In addition, +17V is provided as auxiliary power to the host device.

2.1.3 PRINCIPLES OF PRINTING (GENERAL TO ALL 739 MODELS)

The print mechanism rides on a carriage driven by a DC motor. The printing is performed in the forward direction only, printing up to nine dots per column. Print head actuation is performed by energizing solenoids that drive circular pins, forming dot matrix characters. The paper feed (line feed) rollers are driven by a stepping motor which is capable of forward and reverse line feed; manual and computer controlled. The ribbon drive (AC motor) moves ribbon past the print head at all times except when the carriage actuates the sensor at the leftmost carriage position.

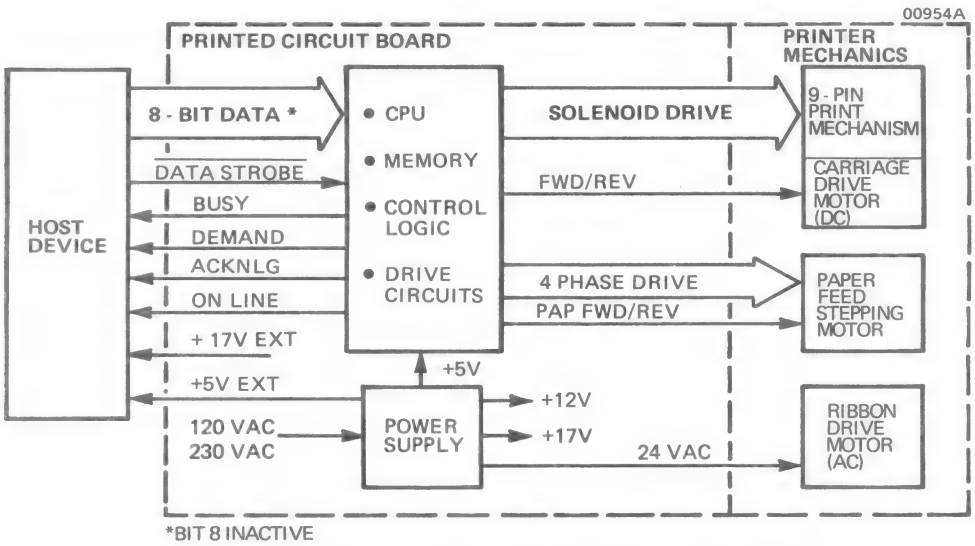


Figure 2-2. 739-1, 739-2 BLOCK DIAGRAM

The printer is capable of printing 80 monospaced characters per line; 10 characters per inch (10 cpi). The monospace matrix is 7x8, in upper and lower-case characters. Monospace descenders (y, g, etc.) do not touch the underline (if used), which is provided by activating the 9th pin for all characters to be underlined (including intercharacter and interword spaces if appropriate). Underline may be turned on or off anywhere within a line and as many times as desired, for all character sets. Monospaced characters may be condensed to 16.7 cpi, resulting in 132 characters per line.

The proportionally-spaced character set is printed in Nx9 (N = 6 to 18) dot matrix. The proportional descenders (y, g, etc.) will run into the underline because the 9th pin is used to form proportional descenders. Proportional text may be right justified by placement of intercharacter and interword spaces generated by the host device.

Average character spacing for proportional is approximately 14 cpi; however, numerals 0-9 are monospaced at 12.5 cpi to allow tabulation. Rather than counting characters to determine a full line, dot positions are counted for the proportional set, 1200 dot positions making a full line. If the host device does not transmit a Carriage Return (CR) to end the line at this point, the logic terminates the line with CR after counting and accepting every column of the character that exceeds a count of 1185, regardless of the width of the character (even an elongated W). The remainder of the truncated word (if this is the case) would begin on the next line. For monospaced 10 cpi, CR occurs at 80 characters, and for condensed (16.7 cpi), CR occurs at 132 characters.

All three basic character sets (proportional, monospaced and condensed) may be elongated beginning anywhere in the line after the host transmits ESC, SO. Elongation is accomplished by simply printing each character column (or space) twice. This results in half as many characters per inch for all character sets, and a wider, bold-appearing character. ESC, SI terminates the elongated characters.

The graphics function is enabled by the sequence ESC % 0 (27, 37, 48 decimal). Graphics are formed using the top six pins only. Each pin is addressable by the host in any combination of pin 1 through pin 6. In the graphics program, LF (Line Feed) commands are converted to one-half line feed, which is equal to six dots in height; thus, a solid graphic pattern can be formed if all six pins are activated in each graphic line. Graphics are terminated by any proper escape sequence such as ESC DC1 (set proportional mode). A table of graphic codes is contained in the 739-1/739-2 Operators Manual.

Line Feed (LF) control codes advance the paper one line at a time. The LF code is a print command; thus, any text prior to the LF code is printed on the present line before the LF is executed. When consecutive LF codes are received, they are counted in a special counter until a character or other non-LF code is received; then the LF's are executed until the count is zero. The printer Busy line is active during printing and LF execution; thus, host transmission is inhibited to avoid noise problems with data transfer.

2.2 SERIAL INTERFACE DETAILED THEORY

2.2.1 RS232C AND CURRENT LOOP CONFIGURATIONS

Models 739-3 and 739-4 are configured for RS232C. Models 739-5 and 739-6 are configured for current loop. Refer to schematic 63680185 in Section 6. The jumper resistor table on sheet 1 shows which jumper resistors are in place for each configuration.

RS232C Operation

When Data Set Ready (J101 pin 6), Data Carrier Detector (pin 8), Data Terminal Ready (pin 20) and Reverse Channel (pin 11) have satisfied conditions for data reception, Received Data (pin 3) passes through jumper resistor R33 and gate ME34 to the data input of the UART (ME3 pin 20). The UART is factory preset to receive 7-bit words (switch pack #1, switch 3 ON) and output Data Bit 8 is grounded at the output connector (J102 pin 17).

Current Loop Operation (-9002)

For 20 mA current loop operation, inverters ME36-6 and ME36-10 have grounded inputs, qualifying gate ME34-12 (without Data Set Ready and Data Carrier Detector). The current (20 mA nominal) is provided by the host and applied to J101 pin 12 (+) and pin 13 (-). Mark = logic 1 = 20 mA; Space = logic 0 = 0 mA. The Mark condition activates opto-isolator ME35 and is converted to TTL (+5V = logic 1) after passing through jumper resistor R34 and gate ME34-12 to the UART (ME3). Refer to 63680185 sheet 4. For current loop operation, jumpers R37 and R31 are factory installed; thus, Buffer Full through jumper R31 causes a Mark (closed loop) condition to occur at J101 pins 14 (+) and 15 (-) which is transmitted to the host. X-ON/X-OFF is not active for 20 mA current loop as configured at the factory. All communication to and from the host is sent through the receive and transmit current loops in full duplex mode (transmit and receive can occur simultaneously).

2.2.2 BAUD RATE; SYSTEM CLOCK

Refer to schematic 63680185 in Section 6. The Baud Rate Generator (ME1) (SH1) divides the 4.9152 MHz crystal frequency by 16 to produce the system clock (ME1 pin 17, FT) whose rate is fixed at 307.2 KHz (3.3 usec) because inputs TA, TB, TC, TD are held at +5V. The baud rate is controlled by switch pack #1, switches 5, 6, 7, 8. Switch 5 is ON (factory preset), grounding the RA input of ME1 to select 9600 baud. The FR output (ME1 pin 3) has a frequency of 16X9600 or 153.6 kHz. This baud rate clock is applied to the TRC and RRC (Transmit Rate Clock, Receive Rate Clock) of the UART (ME3 pins 40, 17); thus, the interface transmit and receive rates are the same (9600 baud).

2.2.3 POWER UP SEQUENCE

Refer to schematic 63680185 in Section 6. When power is turned on, power-up reset circuit R10-C4 (SH4) produces RSTL (Reset Low) at ME32-8 and RST (Reset High) at ME15-8 for 20 msec. RSTL resets the BUFUD FF (1/2 ME27), MWC FF (1/2 ME38) (SH2) and MRC FF (1/2 ME38); loads all zeroes into the Difference Counters (ME20, ME24, ME28) (SH3), clears the Address Counters and Registers (ME9, ME13, ME17, ME7, ME8, ME21), and Cycle Counter (ME5) (SH2). RST resets the UART (ME3) (SH1). Thus, the write and read address lines are zero prior to any write or read operations.

2.2.4 GENERATION OF WRITE AND READ CYCLE STATES

Refer to schematic 63680185 in Section 6. After the power-up reset circuit (R10-C4) times out, the ME5 Cycle Counter (SH2) is enabled and divides the system clock into four binary outputs (QA, QB, QC, QD) which are further decoded into two separate eight-state time frames. The first eight states control write operations (while ME5 QD is low) and the second eight states control read operations (while ME5 QD is high). Thus, write and read operations never occur simultaneously.

2.2.5 WRITE CYCLE OPERATION

Refer to schematic 63680185, sheet 1. When all conditions for data reception are met, Received Data at J101 pin 3 passes through gate ME34 to the UART (ME3 pin 20). When the serial-to-parallel conversion is complete for one code, eight-bit parallel data is developed at ME3 pins 12, 11, 10, 9, 8, 7, 6, 5 and DR (Data Ready) goes high at ME3 pin 19. DR at gate ME41 (SH2) prepares the MWC (Memory Write Cycle) FF to set when both QC and QD of Cycle Counter ME5 transition from high to low. MWC at the U/D inputs of the Difference Counters (ME20, ME24, ME28) prepares an up-count for the Write Cycle. The purpose of the Difference counters is to keep track of the difference between data written into and read out of memory; thus, whenever there is a difference greater than zero the read operation will be qualified by ME28 CO (pin 15) being high. When there is no count (difference = zero) pin 15 goes low to inhibit the setting of MRC (Memory Read Cycle) FF (ME38-9 SH2). Also, the Difference Counters monitor the Buffer Full condition, and the BUFFULL FF (ME27 SH3) is set by 1024+512+256 = 1792 codes written into 2K memory. Buffer Full for 512 buffer is 384 codes (Sheet 3A). BUFFULL is cleared when 256 goes low. J101 pin 11 transmits the buffer status through RC (Reverse Channel) to the host (+ or Space condition on Buffer Full).

The eight bits of data at ME3 (SH1) are multiplexed at ME6 to produce two 4-bit nibbles to be written into RAM (SH2). The 2K buffer RAM is 4096 x 4 bits, thus the lower and upper order nibbles are to be loaded into adjacent locations, forming an 8-bit byte (RAM is thus arranged 2048 x 8 bits). The 512 buffer uses only RAM3 (R40 provides the enable). The ME6 MUX is toggled at the select line (pin 1) by ME5 QC. When QC is low, data bits 1, 2, 3, 4 appear at the 4Y, 3Y, 2Y, 1Y outputs (in complement). ME5 QC (high) switches bits 5, 6, 7, 8 to the ME6 outputs.

Cycle Counter ME5 (SH2) synchronizes all write (and read) operations. MWC FF enables the Memory Write Decoder ME16 to present state information to the MWDF ME12, which produces three important write control signals: Write Enable (low) at pin 7 during State 3 and State 6 to write into the RAM Memory, Write Enable (high) to enable the DIN MUX ME6, and DRR (Data Ready Reset) during State 7 to reset the UART ME3 (SH1) at the end of the write cycle. The Memory Write Decoder is disabled when MWC FF is reset, thus these signals are not active during the read cycle or when no data is received. ME5 QA, QB, QC at Decoder ME11 (SH3) generates Y0 during State 1 to swap the Address Counter and Address Register addresses and Y7 during State 8 to increment the Difference Counter and Address Counter.

All address lines A1-A9 are common to the Address Counter, Address Register and RAM Memory. The Address Counter begins at zero, counts to 511, then wraps around again to zero etc. Since there are 1024 actual locations in each RAM chip, ME5 QC is used to toggle the LSB (A0) of the address input to memory, thus doubling the addressing capability of the Address Counter for each chip. RAM3, 2, 1, 0 are enabled in sequence by AV, AU, AT, AS for the 2K buffer. During the first write cycle, the I/O of memory is a 4-bit input, and data is written into locations zero and one by Write Enable during State 3 and State 6 respectively. Thus, the first 8-bit code is written into two adjacent locations during one write cycle. The write cycle ends with DRR (Data Ready Reset) which occurs at the same time that the MWC FF is toggled to reset by ME5 QD high as QC goes low. DRR clears the data registers of the UART (ME3 pin 13) preparing for the next input code.

2.2.6 ERROR DETECTION, WRITE CYCLE

The ME6 Data Input Mux (SH1) also generates an @ character whenever the ME3 UART detects a Parity Error (PE), Framing Error (FE) or Overrun Error (OE) during data reception. Gate ME34-6 goes high, causing DINMUX (ME6 1Y, 2Y, 3Y, 4Y) outputs to "tri-state". All outputs are pulled up to a logic 1 except data bit 7, which is forced low by enabling Y6 of ME11-9 (during the writing of the 2nd nibble) to pass through ME32 pin 3. The result is the character @ (40 hexadecimal, 100 octal) in complement, written into memory to replace the error character received by the UART.

2.2.7 READ CYCLE OPERATION

Refer to schematic 63680185, sheet 2. The read cycle is entered when Demand and Select from the main logic board are high, the Difference Counter has a count greater than zero, QD transitions from low to high, and MRC FF (Memory Read Cycle) is set by QC going low. The read cycle has the same 8-State time frames as the write cycle. The first four states store the address of the previous operation, fetch the address of the current operation, read the first 4-bit nibble from the I/O of Memory and latch them in the Printer Buffers (ME26, ME25). The second four states are used to read the second 4-bit nibble from Memory and store it in the Printer Buffer, thus, all eight bits are assembled successively so that they can be strobed into the main logic board Input Buffer.

Refer to sheet 3. $\overline{\text{MRC}}$ (low) and MWC (low) prepare the gating circuits for the read operations. MWC (low) at the U/D control input of the Difference Counter (ME20, ME24, ME28) prepares a down-count. Cycle Counter outputs QA, QB, QC at Decoder ME11 produce control pulses Y0, Y3, Y6 and Y7 during the eight read states. Y0 causes the Address Counter and Address Register to swap addresses. Y3 at gate ME23-13 produces a store pulse at the Printer Buffer ME26 pin 10 (SH2) to store the first 4-bit nibble as addressed at RAM3 ME22. Note that the Write Enable input is high during the read cycle, causing the addressed data to appear at the I/O outputs. ME5 QC toggles the A0 Address input to address the second 4-bit nibble. Y6 from ME11 Decoder (SH3) through gate ME23-10 produces another store pulse which stores the second 4-bit nibble in Printer Buffer ME25. This same pulse at the input to Data Strobe FF ME31-5 and the system clock produces the Data Strobe (active low) at J102 pin 1. The 7-bit code (bit 8 is grounded at J102 pin 17 and is not used) is inverted by transistors Q1-Q9 (SH4) to positive true logic and strobed into the main logic Input Buffer. The read cycle ends as Y7 from ME11 (SH3) decrements the Difference Counter by one and increments the Address Counter by one.

2.2.8 BUFFER STATUS

As the serial interface continues to accept data from the host system and transfer parallel data to the main logic PCB, eventually the printer is busy printing, and the read operation is inhibited. In this case, the write operation continues and the difference counters count up.

512 Buffer - Refer to schematic 63680185, Sheet 3A. When the difference is 256, the Buffer Full FF is prepared to set on the following 128 count signal (256+128=384; Buffer Full). Buffer Full (Q NOT) at gates ME19 and ME37 (SH3) forces J101 pin 11 to a Space (+) condition. Thus, RC (Reverse Channel) signals the host that transmissions to the serial interface should cease until more read operations "empty" the buffer. DTR at J101 pin 20 follows the

polarity of RC if SW2-7 is turned OFF; otherwise is held at +V (space). When the 256 line of the Difference Counter goes low, Buffer Full FF is cleared and RC (J101 pin 11) goes to a Mark (-) condition to allow transmissions by the host system.

2K Buffer - Refer to schematic 63680185, Sheet 3. When the difference counters reach 1792 (1024+512+256), the Buffer Full FF is preset by gate ME34. Gates ME19 and ME37 force RC (J101 pin 11) to a space (+) condition. RC signals the host that transmissions to the serial interface should cease until more read operations "empty" the buffer. DTR at J101 pin 20 follows the polarity of RC if SW2-7 is turned OFF; otherwise is held at +V (space). When the difference is counted down to 256 (1024+512+256 low) the Buffer Full FF is cleared through gates ME33, ME23 and inverter ME15. With Buffer Empty, RC is at a mark (-) condition to invite transmissions from the host.

If XON/XOFF is used, Buffer Full high and BUFUD FF ME27 (SH4) (which is reset at this time) cause the exclusive-OR ME19-8 to go low, loading the UART ME3 with DC3 code for XOFF (23 octal). Difference Counter 256 count at ME3 pin 27 provides the logic 1 or logic 0 to produce DC3 or DC1 (in this case, 256 is high for DC3). On the next ME5 QC up-clock, BUFUD FF sets, causing the THRLD input to go high. This triggers the serial transmission of DC3 (XOFF) through the ME37-3 driver to J101 pin 2. The host system's receiving device would then normally inhibit host data transmission until the reception of DC1 (XON). When the interface buffer has fewer than 256 unprocessed codes, Difference Counter 256 count at ME3 pin 27 is low, loading the DC1 code for XON (21 octal). The next ME5 QC up-clock resets BUFUD FF ME27, causing the exclusive OR gate ME19-8 to go high, triggering the UART transmission of DC1 (XON, 21 octal). Current loop transmission of XON/XOFF is not active as configured at the factory, but could be enabled with jumper R32 in and R31 out.

Although the Buffer Full condition signals that the host system should stop transmitting data, a block-transmission from the host may already be in progress. The interface can accept up to 256 additional codes after Buffer Full (for the 2K buffer) without writing over previous codes or otherwise losing data. The 512 buffer allows 128 additional codes. The last write cycle resets the No Overflow (NOVF) FF ME31-9 (SH3), inhibiting the setting of MWC FF and the write cycle is disabled until the Difference Counter decrements to 256.

When the transmission from the host terminates, the read operation continues until the interface buffer is equal to zero. Difference Counter ME28 pin 15 goes low, inhibiting the setting of MRC FF ME38 (SH2) and the read operation ceases. The write-read sequence resumes when serial data is received and Select and Demand are active.

2.3 DETAILED THEORY DESCRIPTION

2.3.1 MICROPROCESSOR

Refer to Figure 2-4. The microprocessor (U3; 8049) controls all communication on the data/address bus, communication to the host (or serial IF PCB) and reception of data. The basic clock (6 MHz) provides the time base for all timing pulses, motor steps and sequences used in the printer. U3 contains 128 bytes of RAM and a storage capability of 255 consecutive Line Feed commands. An Auto LF load resistor is provided so that CR (Carriage

Return) codes are followed by a Line Feed without additional command when Auto LF is enabled on switchpack S5.

Principle input signals to U3 are as follows: $\overline{\text{RESET}}$ is used to start the power-up and initialization routines. RTP (Ready to Print) is true at the Test 1 input when the carriage is positioned for printing the first character of the line near the left margin. The Busy FF (Q NOT is DEMAND) is applied to the Test 0 input to indicate storage of new data to be processed. The EA (External Access) input is tied to a Logic 1, directing program memory fetches toward the external memory (U13 ROM). If a masked 8049 ROM containing program is installed, the EA input is pulled to ground by a zero ohm resistor, and the resident program of the 8049 is used instead of the external memory. This description assumes external program memory. COLSENSE from the carriage sets the Interrupt FF at the $\overline{\text{INT}}$ input. The rotating magnet on the carriage generates 100 COLSENSE pulses per inch, 800 per line. Internal to U3, the software converts two COLSENSE pulses to three Column Interrupts when processing proportional, condensed and graphics (Figure 2-3). This provides 1200 character dot columns (positions where pins may or may not be driven depending on the text). The 10 cpi monospaced character set uses 800 columns (80 characters); thus, the special conversion is disabled for 10 cpi monospaced.

01053

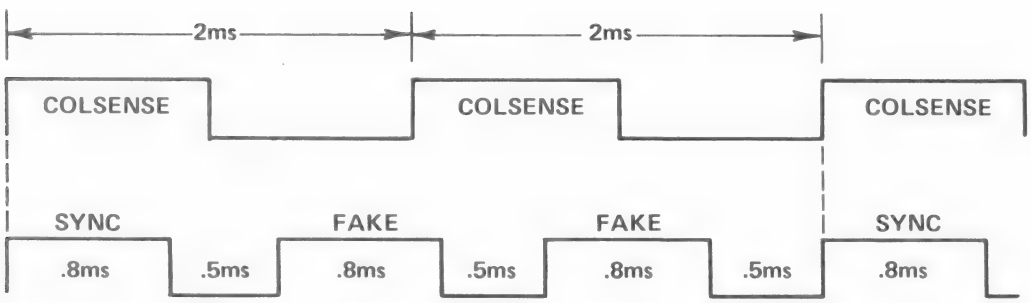


Figure 2-3. SOFTWARE INTERRUPT TIMING (PRINT STROBE)

Principle outputs from U3 are as follows: U3 uses DB0-DB7 as a bi-directional bus for transferring data, address and column patterns for pin driving. The program residing in U13 is transferred to the Microprocessor over this bidirectional bus. Pin #9 from P25 of U3 carries 9th pin data for underlining all character sets and for descenders of the proportional set. High order bit addressing of U13 and U18 is provided by A8910 when 8 bits of address are not adequate. A8910 are the P20, P21 and P22 outputs of U3. ALE (Address Latch Enable) is sent to U9 and U18 to latch the address bits. The bus is then available to accept the data being addressed. ALE also clocks U14 Address Latch to hold address to U13 which has no latch capability. $\overline{\text{PSEN}}$ (Program Store Enable) is developed shortly after ALE during a program memory fetch and provides an $\overline{\text{OE}}$ (Output Enable) for U13, placing the contents of the location addressed onto the bus. $\overline{\text{CLMPEN}}$ (Clamp Enable) pulse triggers

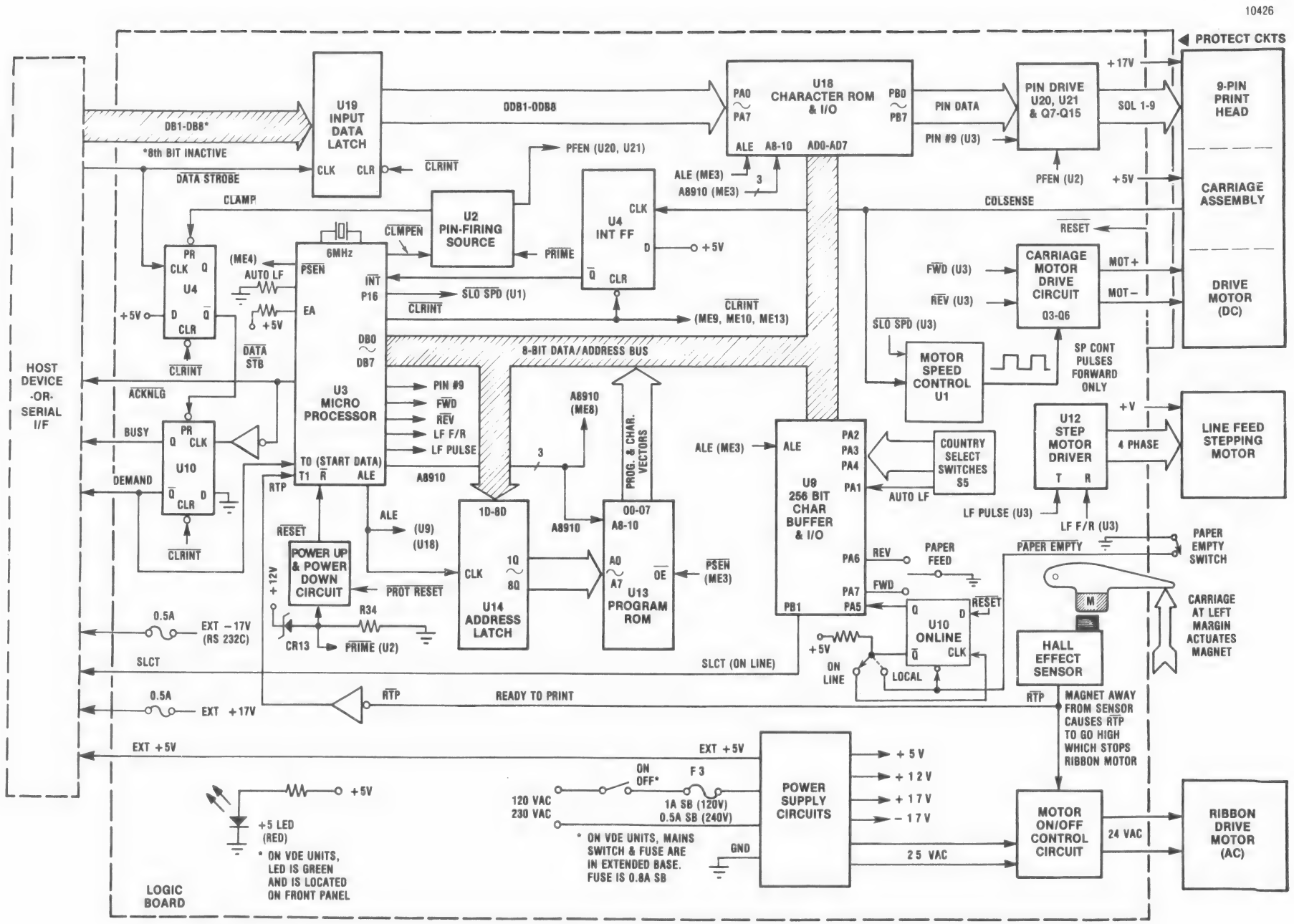


Figure 2-4. DETAILED BLOCK DIAGRAM

U2 after initialization. This enables U2 to current source the pin drivers. CLRINT (Clear Interrupts) resets U19 Latch, the Data Strobe FF and Busy FF. FWD and REV (P11 and P12 of U3) control the direction of the carriage drive motor. LF FWD/REV (P26 of U3) controls the direction of the Line Feed stepping motor. LF FWD/REV low at U3 allows normal (forward) line feed. LF PULSE is the line feed Motor Step pulse (P27 of U3) generated by the internal timer. Eight LF PULSE pulses equal one line feed (one-sixth inch of paper). At the LF PULSE rate of 100 pps, paper moves at 2 inches per second.

Microprocessor outputs not shown in Figure 2-3 are found on print 63680148 and are as follows: IO/M (P26 of U3, same line as LF FWD/REV) selects the I/O or Memory function of U9 and U18. IO/M (low) selects RAM in U9 and ROM in U18. CE (Chip Enable) for U18 is output at P23 and CE for U9 is output at P24. RD (Read the bus) is an output strobe to enable data onto the bus for the microprocessor to read. At U9, RD allows the microprocessor to read a print character code from RAM or to examine switch settings at Port A. At U18, RD allows the microprocessor to read a character column from ROM for printing or to accept new data from Port A (ODB1-ODB8). WR (Write the bus) is an output strobe used to write data into an outboard memory. For U9, WR writes data into RAM or Port B. For U18, WR writes pin driving data onto Port B.

2.3.2 PROGRAM MEMORY

The U13 ROM contains the initialization routine, all program for this system and vectors (starting addresses) for character matrix data contained in U18. The ROM has 11 address lines, 2048 locations and an 8-bit data output bus. In this circuit, CE (Chip Enable) is actively tied to ground and the data output is enabled by PSEN at the OE input (pin 20). The 8 LSB of address are latched to the A0-A7 inputs by U14 (clocked by ALE). The three MSB are A8910 (P20, 21, 22 of U3).

2.3.3 INPUT DATA LATCH

The Input Data Latch stores each byte of input data as it is transmitted by the host device. The code format is 7-bit ASCII, positive true logic. The 8th bit is inactive in this system. The host transmits DB1-DB7 for approximately 3 microseconds and a DATA STROBE of about 1 microsecond, transmitted in the middle of the data window. The trailing edge (up-clock) of the strobe clocks the data into U19. The data is available at the 1Q-8Q outputs until CLRINT clears the latch. DATA STROBE also sets the Data Strobe FF, which presets the Busy FF. The T0 input to the microprocessor goes low, and when the program tests for zero at this input, the new data is processed.

2.3.4 CHARACTER BUFFER AND I/O

U9 contains a 256 x 8 bit RAM that stores characters not yet printed. All addressing and data transfers are performed on the bi-directional bus AD0-AD7. ALE (Address Latch Enable) is used to latch the Address, CE (Chip Enable) and IO/M inputs. When CE is low, the AD0-AD7 input lines go to a high-impedance state so that this chip does not influence the bus. Latching occurs on the trailing edge (down-clock) of ALE. DATA is written into or read from U9 depending on the status of WR or RD inputs. IO/M determines whether the RAM or one of the ports is written or read. If IO/M is low, RAM is selected.

RESET (high) clears all registers and ports during power up, programming the C/SR (Command/Status Register) bits 0 and 1 so that Port A and Port B are inputs. Later in the initialization routine, Port B is instructed to be an output port. In this system, Port A (PA0-PA7) is used only as an input for examining switches. The ON LINE/LOCAL switch (and paper empty status) is input at PA5 and is written out at PB1 as SELECT during a WR cycle by the microprocessor. Data cannot be sent by the host device unless SELECT (and DEMAND) is active, as the initialization program hangs up in a tight loop until SELECT is high. In the LOCAL mode, the PAPER REV/FWD switch controls the direction of the Line Feed stepping motor that drives the paper feed roller. Pressing the switch momentarily produces one line feed in that direction. Holding the switch for more than one-half second produces continuous line feed for as long as the switch is held.

2.3.5 CHARACTER ROM AND I/O

U18 contains an EPROM (Erasable, Programmable Read-Only Memory) of 2048 x 8 capacity in which the character column data reside. Only eight pin positions (vertical) can be stored; thus, for underlining and for proportional descenders, 9th pin data is transmitted by the Microprocessor during the print operation. The starting address for each character is indicated by vectors contained in U13 Program ROM. The bi-directional bus AD0-AD7 is used to transfer data and addresses. Three additional bits A8-A10 are used as the high order address to the ROM. $\overline{CE}$ (Chip Enable, low) is actively tied to ground and CE (high) is used to enable U18. When CE is low, the chip is de-selected and AD0-AD7 go to the high-impedance state. The selection of the U18 ports (PA, PB) and the direction of data are accomplished by addressing and writing two independent 8-bit registers, DDR A and DDR B (Data Direction Registers A and B). Port A is selected by AD0 and AD1 low; Port B is selected by AD0 high and AD1 low. DDRA is addressed by AD0 low, AD1 high. DDR B is addressed by AD0 high, AD1 high. Although individual lines of each port may be written as input or output, all Port A lines are new data inputs from the host device and all Port B lines are pin drive outputs to the ME14-ME15 high-voltage drivers. All ones written into a DDR make that port an output and all zeroes make that port an input. The DDR's cannot be read. ALE latches the address lines AD0-AD7 and A8-A10, CE, $\overline{CE}$ and IO/$\overline{M}$ on the trailing edge (down-clock). $\overline{RD}$ low reads ROM or an I/O port out to the bus, depending on IO/$\overline{M}$. IO/$\overline{M}$ low reads ROM and IO/$\overline{M}$ high reads Port A (new data). Because $\overline{IOR}$ is tied to Logic 1, RD high causes AD0-AD7 to go to a high impedance. $\overline{IOW}$ low (with CE high) writes Port B with pin drive data, assuming AD0 high was previously latched. With $\overline{IOW}$ active, the state of IO/$\overline{M}$ is ignored. RESET high (occurs during power up) programs all port pins to be inputs.

2.3.6 PIN-FIRING SOURCE AND CLAMP

The NE555 is normally used as an RC timer circuit. In the 739, U2 Pin Firing Driver Control provides a driving current for the nine solenoid drivers Q7-Q15. When microprocessor U3 delivers $\overline{CLAMPEN}$ (800 usec) with Pin Data present at the U20-U21 open collector drivers, U2 develops PFEN (Pin Fire Enable) which turns the Q7-Q15 transistors on for 800 microseconds. Those transistors with positive pin data will fire the solenoids (SOL1-SOL9) as appropriate. After the 800 microseconds of solenoid current, return springs withdraw the pins to the home position in preparation for the next firing.

U2 also monitors the +12V power supply for eventual power down, or extended power dip. Refer to Paragraph 2.3.2 for the power-down description.

2.3.7 MOTOR DRIVE AND SPEED CONTROL

The print carriage is driven on a rack by a reversible DC motor through a reduction gear train. Motor direction is controlled by $\overline{\text{FWD}}$ and $\overline{\text{REV}}$ from the microprocessor. The basic power source is +17 VDC, and heavy-current polarity switching is provided by power transistors Q3-Q6 connected in complementary-symmetry. These four transistors effectively reverse the motor connection to the +17V supply; Q3 and Q6 conducting when $\overline{\text{FWD}}$ is active, Q4 and Q5 conducting when $\overline{\text{REV}}$ is active.

The Motor Speed Control is a closed-loop feedback circuit for setting and regulating the forward carriage speed. The circuit compensates for variations in temperature and line voltage. Refer to schematic 63680193 for the following description.

The COLSENSE pulse rate (frequency) from the carriage is proportional to motor speed; thus, COLSENSE is used as the tachometer input to Motor Control chip U1. The differential (+ and -) tachometer inputs are provided by the U11 inverter. The rate of COLSENSE pulses is 1 KHz (one pulse every msec) at the carriage speed of 10 inches per second. The COLSENSE pulses trigger a pulse generator inside U1. The resulting constant-amplitude pulses are partially integrated by R28-C21, the pulsating DC applied to the U1 comparator (-MD). The reference input (+MD) to the comparator is a steady DC level from potentiometer R25 (Speed Adjust). $\overline{\text{SLOSPD}}$ is active low for graphics, condensed and proportional, reducing the forward speed by sinking the high leg of R25 to half normal voltage. Return speed is always 10 inches per second. The comparator outputs a modulated DC waveform whose duty cycle is about 60% at the motor speed of 10 inches per second and about 30% at five inches per second (for graphics, condensed, expanded and proportional). This pulse-width modulated waveform (SP CONT PULSE) is applied through the U6 driver to the power transistor Q3, which intermittently applies +17V to the MOT+ terminal (+17V is inhibited by $\overline{\text{SP CONT PULSE}}$). Ground return from the MOT- terminal is provided by Q6, which is on when $\overline{\text{REV}}$ is inactive.

If the motor tends to slow down, COLSENSE pulses are less frequent, resulting in a greater duty cycle (more ON time than OFF) from the comparator; thus, the motor speeds up to normal.

2.3.8 LINE FEED MOTOR CIRCUIT

The Line Feed motor is a reversible, 4-phase stepping motor. 10-ms rep rate pulses are provided by the micropocessor; 8 LF PULSE pulses produce one-sixth of an inch of paper feed. Forward and reverse stepping are controlled by LF $\overline{\text{FWD}}$/REV (P26 of U3). LF $\overline{\text{FWD}}$/REV low at U6-11 provides forward line feed. P26 is time shared with IO/$\overline{\text{M}}$ control of U9 and U18. The field of the stepper motor is supplied with +17V through transistor Q18 and resistor R52 (5.6 ohms) and (pulsed) ground sink is provided by the Q1-Q4 outputs of U12. The rotor is a multipole permanent magnet whose poles are spaced so that 8 LF PULSES produce one line feed by turning the drive roller one-sixth inch.

2.3.9 RIBBON MOTOR CONTROL CIRCUIT

The ribbon motor runs almost continuously, stopping only when the carriage actuates the Hall effect sensor by moving the magnet away from S1 (UGN 3013) at the left margin. The control works as follows: while the magnet is against the sensor, $\overline{RTP}$ is low, which turns Q2 on. This allows gate current for Q1 (silicon-controlled rectifier) which provides a conductive bridge for diodes CR1-CR4. Two diodes conduct with each alternation from T1; either CR1+CR4 or CR3+CR2. Thus, 24 VAC is applied to the AC motor (the diodes do not rectify, they are switches). When the magnet is moved away from the sensor, $\overline{RTP}$ goes high and Q2 shuts off, removing gate current from Q1, opening the bridge and stopping the motor. If the carriage moves forward again to prepare for another line of printing, the magnet actuates the sensor, $\overline{RTP}$ goes low and the microprocessor prepares the print routine.

2.3.10 POWER SUPPLY CIRCUITS

The power supply output voltages are +5V regulated, +12V regulated, +17V unregulated and -17V unregulated. The -17V is used for the RS232C Serial Interface only.

(+17V, -17V Power Supplies) - Transformer T1 steps the line voltage (120V, 60 Hz; 230V 50 Hz) down to 25 VAC center-tapped for full-wave rectification by CR5, CR8 (+17V) and CR6, CR7 (-17V). Large filter capacitor C11 (10,000 uF) provides pre-filtering for the +12V regulator and acts as the dynamic current source for the pin-firing solenoids. Capacitor C10 filters the -17V output, which is used only for RS232C Serial Interface power through fuse F1 (0.5ASB).

(+12V Power Supply) +17V is applied to regulator chip VR2 whose output is regulated at +12V. C15 is the post-filter capacitor.

(+5V Switching Power Supply) +17V is applied to R70 (.075 ohms, 1W), and all current supplied by the +5V output passes through R70, Q19 (series pass element) and inductor L3. Switching power regulator chip U16 monitors current at pins 13 and 14 (IR drop of R70) and provides current limiting protection. The nominal switching rate of U3 is approximately 2.2 kHz. Output voltage is monitored at C14 with C13 +R63 providing negative feedback to U16 pin 10 (-comparator). Transistor Q19 is switched at its base through R73 every 450 microseconds. If +5V tends to increase, the negative feedback reduces the switching frequency, thereby reducing the charging rate of filter capacitor C14, lowering the output voltage. Inductor L3 removes most of the switching transients, aided by C16. CR48 clamps the negative polarity flyback from L3, protecting Q19 from transients.

2.3.11 FLYBACK PROTECT CIRCUIT

Refer to drawing 63680193, Sheet 3. An inductive voltage is developed across the solenoid windings when they are energized by the drive transistors Q7-Q15. This transient voltage occurs as the 800 microsecond pin-firing pulse (PFEN) times out. Polarity-steering diodes CR38-CR46 and zener diodes CR27-CR35 absorb the inductive voltage which otherwise would be applied to the drive transistors. The transient voltage could puncture or overheat the transistors if the flyback protect circuit was not present. Additionally, 2.5 ampere fuses in series with the solenoids provide burnout protection in the event of driver circuit failure.

2.3.12 PRINT SOLENOID PROTECT CIRCUIT

Refer to drawing 63680193, Sheet 3. When a solenoid is normally driven, the drive transistor (Q7-Q15) grounds the cathode of gating diode (CR14-CR21) through one of the fuses (F4-F12). The grounded diode shuts off Q16 for 800 microseconds (PFEN) which causes Q17 to turn on. R61 discharges C28 slightly through Q17, but after the 800 microsecond pulse, C28 charges back up to normal. If a solenoid receives constant current due to a circuit failure, R61 discharges C28 below the threshold level (+1.4V) at U17 pin 10 and PROT RESET is generated at U17 pin 13 (low). This resets the microprocessor until the problem is cleared.

2.3.13 MOTOR STALL PROTECT CIRCUIT

Refer to drawing 63680193, Sheet 3. COLSENSEB pulses charge capacitor C29 to a level more positive than the reference (+1.4V) on U17 pin 6. This allows +5V through R64 and CR47 to clamp U17 pin 11 at a more positive voltage than reference at U17 pin 10. Thus, PROT RESET stays inactive (high) while the carriage is moving, producing COLSENSE pulses. If the motor stalls, the COLSENSE pulses cease, and R65 discharges C29 to a level lower than reference. U17 pin 13 goes low, activating PROT RESET, resetting the microprocessor. Under this condition, motor polarity is reversed and the carriage is sent to the left margin (back to the RTP switch).

2.4 POWER UP/DOWN ROUTINES

2.4.1 POWER UP/INITIALIZE ROUTINE

Refer to Figure 2-3 and print 63680193, SH2. When the power switch is turned on, the +5V logic supply gets up to Logic 1 (approximately +3V) in a few milliseconds. A R-C delay provided by C4 (10 uF) and R4 (12K ohms) holds a low on pin 3 of inverter U8 for 120 milliseconds. Inverter U5-8 holds the RESET input to microprocessor U3 low. U8 provides a high level to the RESET inputs of U9 and U18. The CLAMP from U2 is low, disabling the solenoid drivers and presetting Data Strobe FF and Busy FF to inhibit host data. After the power-up reset circuit C4-R4 times out, the microprocessor performs the initialization routine which includes the following: disable column interrupt with CLRINT, which also clears the Input Data Latch U19 and Data Strobe FF, releasing the preset on the Busy FF; addressing the DDR's and CSR's of U9 and U18 to set up the ports; prevent pin firing; select the primary character set (10 cpi monospaced); clear 8049 memory and move the pointer to the top of RAM; clear the data buffer in U9; check for print head at left margin (RTP) and home it if required; check for ON LINE at U9 (loop here if LOCAL) and prepare for host data.

2.4.2 POWER DOWN ROUTINE

Whenever the AC line voltage takes an extended dip, or if power is lost to the printer for any reason, the printer circuitry prevents pin driving and data transmission from the host device as follows: The +12V applied to zener diode CR13 falls below the zener voltage and resistor R34 (270 ohms) generates PRIME (low) before the +5V logic supply falls below logic 1. PRIME makes CLAMP go low, removing solenoid driver bias (disabling pin driving). CLAMP also presets Data Strobe FF which sets Busy FF, inhibiting data from the host device. The microprocessor (U3), U9 and U18 are also reset. All print codes in U9 data buffer are lost. When the host device polls the printer status, SLCT (ON LINE) is low and EXT +5V is low, indicating power down at the printer.

2.5 INPUT DATA CYCLE

Refer to Figure 2-3. Data is sent by the host device (or Serial Interface) when SLCT is active and ACKNLG has set DEMAND to invite data. The character set has been selected by power up or by the host transmitting ESC, DC1; ESC, DC3 or ESC, DC4. The host sends a 7-bit ASCII code and a strobe. The code is latched at U19 and made available at U18, Port A. The strobe alerts the 8049 microprocessor that a new input code is available, so the 8049 calls the code in, using the 8-bit bidirectional bus. BUSY is set to inhibit transmissions from the host until this code is completely processed. The 8049 strips the 8th bit, ignores NULL codes (0000000) and treats deletes (1111111) as NULL codes. No operation takes place for NULL's and the next data is called in.

The 7-bit ASCII code is decoded in the 8049 to determine if it is a control code, in this sequence: BS, LF, CR, ESC, SO and SI. If not a control code, the dot column width of this character or space is determined, considering whether Elongation is active and whether the character is 10 cpi, 16.7 cpi or proportional. The character count is also kept (except for proportional) so that the Buffer Full condition can be determined to end the line if the host neglects sending CR. Thus, the dot column width is added to the column count and the 7-bit ASCII code is sent to the 8156 RAM (U9) where it is stored (buffered). Note that some control codes (SO, SI) are immediately buffered and the next code is called in. Buffered codes comprise the line to be printed, when appropriate.

If an ESC control code is decoded, an Escape sequence is recognized and the next code is called to be examined. For example, if the code following ESC is SO, the Set Elongated Characters sequence is decoded and this condition is set in the 8049. Characters and spaces following this sequence will be elongated, the column count being doubled for each character and space. If the code following ESC is decoded as a character whose dot column width is less than 7, a Justification Space sequence is recognized (ESC, 1 thru ESC, 6). The column count is increased by the designated space and the code is buffered as a character.

Graphics is entered by the sequence ESC, %, 0. Each graphic code is binary pin data plus 32 decimal (20 hex.). 594 graphic codes comprise a full line (8 inches, 203 mm). If 594 graphic codes are sent in a line, the software forces a CR (Carriage Return) code. With Auto Line Feed enabled, an automatic one-half line feed occurs to prepare for the next graphic line. In graphics, LF codes sent by the host are also converted to one-half line feed. Graphic codes are contained in the Operators Manual.

When CR is decoded, or when Buffer Full occurs, the program calls the Print Routine. Note that all other control codes which are terminators also call the Print Routine. For a list of control codes and their functions, refer to the Operators Manual.

2.6 PRINT CYCLE

The Print Cycle is entered when a CR code is received or a Buffer Full condition exists. Any terminator control code will also result in the program switching from the Input Data Cycle to the Print Cycle. Assuming that the carriage is at the left margin and has stepped forward to generate RTP (Ready to Print), the print head is in position to drive pins to form characters. A line of characters, spaces and control codes is held in the Print Buffer (U9; 8156) in the form of 7-bit ASCII codes.

The first 7-bit ASCII code is transferred from the Print Buffer to the 8049 over the 8-bit bidirectional bus. The character is decoded to determine whether it is a control code (such as an ESC, DC3 sequence to select 10 cpi) or a printable character. If a printable character such as upper case A, a separate table must be consulted depending on whether the character set is monospaced or proportional. The 8049 adds an offset to the ASCII code and addresses the 2716 ROM (U13) to obtain the vector for this character. The vector is the starting address of the pin data for the character. The pin data resides in U18 ROM in the form of vertical columns, each column in an adjacent location. For proportional characters, both the starting and ending addresses must be determined because the width format is not constant (N=6 to 18 dots wide).

To print characters, the 8049 addresses the U18 ROM to transfer the pin data over the bidirectional bus. After possible minor reconstruction, each sequential column of data is transmitted back over the bus to drive the pins to form the character as the print head moves to the right. Synchronization for pin drive is provided by COLSENSE pulses from the carriage. For spaces, no pins are driven. If proportional descenders require 9th pin drive, the vertical position of the column within U18 ROM is shifted up by one dot so that the 9th pin data is sent to the 8049 on the 8th data line. Characters with descenders have no ascenders, so no data is lost in the vertical shift. In the 8049, the column is shifted back down and the 9th pin is transmitted separately but synchronized with the 8-bit drive.

Underline data is not contained in U18 ROM as a character; continuous 9th pin drive is issued directly from the 8049 while underline is active. Underline and 9th pin descenders merge as a single 9th pin drive. Only the vertical rule (with underline active) drives 9 pins simultaneously.

Carriage speed for 10 cpi monospaced is approximately 10 inches per second, because SLOSPD is not active for 10 cpi. When proportional and 16.7 cpi monospaced characters are being printed, the additional print strobes (described previously) are generated from COLSENSE pulses (3 print strobes from 2 COLSENSE pulses) so that more characters per inch are printed although the carriage moves forward at a constant 5 inches per second (SLOSPD is active). Carriage return speed is 10 inches per second.

Graphics are printed using only the top six pins, which is equivalent to one-half line feed in height. Thus, when a graphic line feed (one-half normal LF) is performed, the subsequent graphic line abuts the graphic line above, allowing a solid pattern if desired. Like proportional and expanded, graphics are printed at five inches per second in the forward direction, as SLOSPD is active.

Whenever a printed line is interrupted by an ESC, FS (Half Line Feed) or similar control code, the carriage always returns to the left margin sensor and moves forward, counting COLSENSE pulses to reach the appropriate position to print the next "line". This is done to obtain the greatest positional accuracy because overshoot caused by carriage momentum is washed out in this manner.

SECTION 3

MAINTENANCE AND TROUBLESHOOTING

3.1 GENERAL

This section contains information on maintaining and troubleshooting the printer. Routine preventive maintenance is contained in the Operators Manual. Troubleshooting procedures contained in this section aid in isolating malfunctions to defective assemblies or required adjustments.

3.2 SERVICE CLEANING AND LUBRICATION

This cleaning and lubrication procedure should be performed by qualified service personnel whenever the printer requires servicing or repairs which require the cover assemblies to be removed. The procedures should be performed prior to detailed service and repair procedures as some malfunctions can be caused by dust, ribbon chaff, paper chaff, residue build-up, or inadequate lubrication.

1. Remove the printer cover assemblies per instructions in Operators Manual.

2. Visually inspect the interior of printer for loose wires, connectors, and hardware, chaffing of cables, and badly worn or damaged parts.

3. Remove the Mechanism Assembly per paragraph 5.3 and set it to one side.

4. Using a soft bristle brush sweep away the paper and dust residue from the printer base and printed circuit board.

5. Clean the print head and carriage assembly using a soft bristle brush to remove dust and residue.

6. Gently remove all dried ink from the front of the print head using a soft, clean, lint-free cloth.

7. Clean contaminated parts of the rest of the mechanism assembly using a freon-moistened lint-free cloth. Pay particular attention to the carriage shafts and the paper roller end-plate bushings.

8. Clean the carriage shafts by applying several drops of lubricating oil to a soft, clean lint-free cloth, then moving the print head to the left side of printer and lightly rubbing the shafts to remove residue build-up. Move print head to the right side of the printer and clean the left side of the shafts.

9. Clean the paper drive roller and the end plate bushings using a soft, clean, lint-free cloth, then apply one drop of light lubricating oil to both paper roller end plate bushings. Cycle the paper roller using the thumbwheels to allow the oil to seep into the bushings.

10. Reassemble the printer and continue with service procedures. After completion of service, clean all external surfaces using a mild detergent and a soft, clean, lint-free cloth.

3.3 TROUBLESHOOTING

Table 3-1 list some malfunctions which may occur, the probable causes, and the remedies which may be performed by qualified service personnel. The procedures referenced in the detailed troubleshooting chart should be performed by qualified service personnel who have been trained to maintain and repair complex electronic and electromechanical equipment.

Table 3-1. Detailed Troubleshooting Chart

TROUBLE	PROBABLE CAUSE	REMEDY
Printer on, but inoperative.	Paper Out Switch needs adjustment.	Adjust per paragraph 4.6.
	Fuse blown.	Replace Fuse.
	Defective Serial PCB.	Replace Serial PCB per paragraph 5.7.
	Defective Logic PCB.	Replace Logic PCB per paragraph 5.6.
Head drags (wide smudge on paper).	Head gap improperly adjusted.	Adjust printer head gap. (See paragraph 4.3).
	Defective head-carriage assembly.	Replace defective head-carriage assembly. (See paragraph 5.5).
Light smudge under print line.	Head gap improperly adjusted.	Adjust printer head gap. (See paragraph 4.3).
	Defective head-carriage assembly.	Replace head-carriage assembly. (See paragraph 5.5).
Tears or creases in paper (jams).	Head gap improperly adjusted.	Adjust printer head gap. (See paragraph 4.3).
	Defective head-carriage assembly.	Replace head-carriage assembly. (See paragraph 5.5).
Print too light.	Head gap improperly adjusted.	Adjust printer head gap. (See paragraph 4.3).
	Worn out or defective ribbon.	Replace ribbon. (See ribbon loading procedure in Operators Manual).
	Defective head-carriage assembly.	Replace head-carriage assembly. (See paragraph 5.5).

Table 3-1. Detailed Troubleshooting Chart (cont'd)

TROUBLE	PROBABLE CAUSE	REMEDY
Left hand margin wanders.	Defective Logic PCB.	Replace Logic PCB. (See paragraph 5.6).
	Defective mechanism assembly.	Replace mechanism assembly. (See paragraph 5.4).
Prints too slowly.	Printer requires general cleaning and lubrication.	Clean and lubricate printer. (See paragraph 3.2).
	Print speed improperly adjusted.	Adjust print speed. (See paragraph 4.5).
	Defective Logic PCB.	Replace Logic PCB. (See paragraph 5.6).
	Defective head-carriage assembly.	Replace head-carriage assembly. (See paragraph 5.5).
	Defective mechanism assembly.	Replace mechanism assembly. (See paragraph 5.4).
Prints erratically (missing dots).	Defective 9-wire head ribbon cable assembly.	Replace 9-wire head ribbon cable assembly.
	Defective Logic PCB.	Replace Logic PCB. (See paragraph 5.6).
	Defective print head.	Replace head/carriage assembly, per 5.5.
Same dot(s) always missing.	Defective ribbon cable.	Replace 9-wire head ribbon cable assembly.
	Defective Logic PCB.	Replace Logic PCB.
Print nothing but @ characters.	Switch settings on serial interface PCB.	Refer to Operators Manual for settings.

Table 3-1. Detailed Troubleshooting Chart (cont'd)

TROUBLE	PROBABLE CAUSE	REMEDY
Line feed operates improperly.	Printer requires general cleaning and lubrication.	Clean and lubricate printer. (See paragraph 3.2).
	Line feed stepper belt/ pulley improperly adjusted.	Adjust belt tension or tighten pulley.
	Defective mechanism assembly.	Replace mechanism assembly. (See paragraph 5.4).
	Defective Logic PCB.	Replace Logic PCB. (See paragraph 5.6).
Carriage emits thumping noise while printing.	Printer requires general cleaning and lubrication.	Clean and lubricate printer. (See paragraph 3.2).
	Defective carriage molded rack assembly.	Replace mechanism assembly (See paragraph 5.4).
	Defective head-carriage assembly.	Replace head-carriage assembly. (See paragraph 5.5).
	Defective mechanism assembly.	Replace mechanism assembly. (See paragraph 5.4).
No ribbon movement.	Ribbon drive motor connector unplugged.	Check for proper connection.
	Defective ribbon drive motor.	Replace body cover assembly.
	Defective Logic PCB.	Replace Logic PCB. (See paragraph 5.6).

SECTION 4

ADJUSTMENTS

4.1 INTRODUCTION

Certain malfunctions and marginal operation may require that the printer be adjusted. Adjustment should also be performed whenever an affected part is replaced in the printer. The following adjustment procedures are contained in this section.

- Printer Head Gap Adjustment
- Rotor/Hall Effect Sensor Clearance Adjustment
- Print Speed Adjustment
- Paper Out Switch Adjustment

All of the procedures contained in this section are performed with the printer cover assemblies removed. Refer to the Operators Manual for the procedure for removing the printer cover assemblies, and to Section 5 for other removal procedures as required.

Only the Print Speed adjustment is performed with power applied to the printer. As this procedure is performed with the cover assemblies removed, care must be taken.

WARNING

Care must be taken when adjusting the printer with the covers removed and power applied to the printer as injury can result from contact with moving parts of the printer or areas within the printer where hazardous voltages are present.

Before performing any adjustment procedure contained in this section, read the procedure carefully to ensure that it is understood, that the appropriate tools and accessories are available, and that care is exercised when performing the adjustment. Return all ground wires to their proper connectors when reassembling covers.

4.2 TOOLS REQUIRED

The procedures contained in this section require the following tools:

Tools

- 1/4 inch flat tip screwdriver
- 1/4 inch nut driver
- 5/8 inch nut driver
- Ohmmeter
- 3/8 inch ignition wrench
- No. 1 Phillips screwdriver
- .004 feeler gage
- .005 feeler gage
- .014 feeler gage
- 2 mm Allen wrench
- .050 Allen wrench

4.3 PRINTER HEAD GAP ADJUSTMENT

1. Remove the printer cover assemblies and remove the mechanism assembly from the base.

2. Carefully move the print head to the center of the printer mechanism. Handle the carriage by the sturdy casting area above the carriage rack.

3. Refer to Figure 4-1. Place the print head release lever in position 1 and insert a .014 inch feeler gage between the nose of the print head and the platen.

4. Loosen the set-screw located on the left side of the head carriage assembly using a 2 mm Allen wrench.

5. Adjust the cam-bushing adjusting nut (using a 3/8" open-end wrench) located under the left side of the head-carriage assembly until the .014 inch feeler gage slips easily between the print head nose and the platen.

> NOTE
> Ensure that the print head release lever is maintained in position 1 during this adjustment.

6. Tighten the set-screw loosened in step 4.

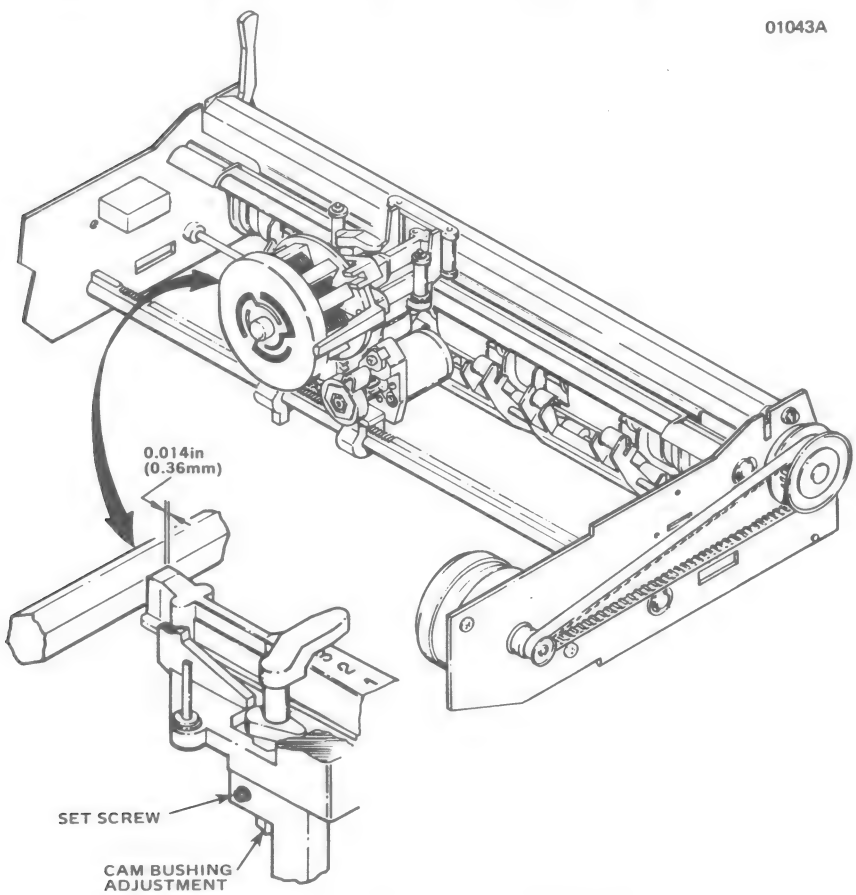


Figure 4-1. HEAD GAP ADJUSTMENT

4.4 ROTOR/HALL EFFECT SENSOR CLEARANCE ADJUSTMENT

1. Remove printer cover assemblies and remove mechanism assembly from printer base.

2. Refer to Figure 4-2. Loosen the Hall effect sensor mounting screw on the head carriage assembly using a No. 1 Phillips screwdriver.

3. Insert a .005 feeler gage between the sensor and the magnetic rotor.

4. Move the sensor against the feeler gage until the gage can be moved with slight friction, then tighten the mounting screw.

5. Insert a .004 feeler gage between the sensor and the magnetic rotor. The gage should fit loosely.

6. Carefully move the head carriage assembly and observe the rotor. The rotor should rotate without touching the sensor.

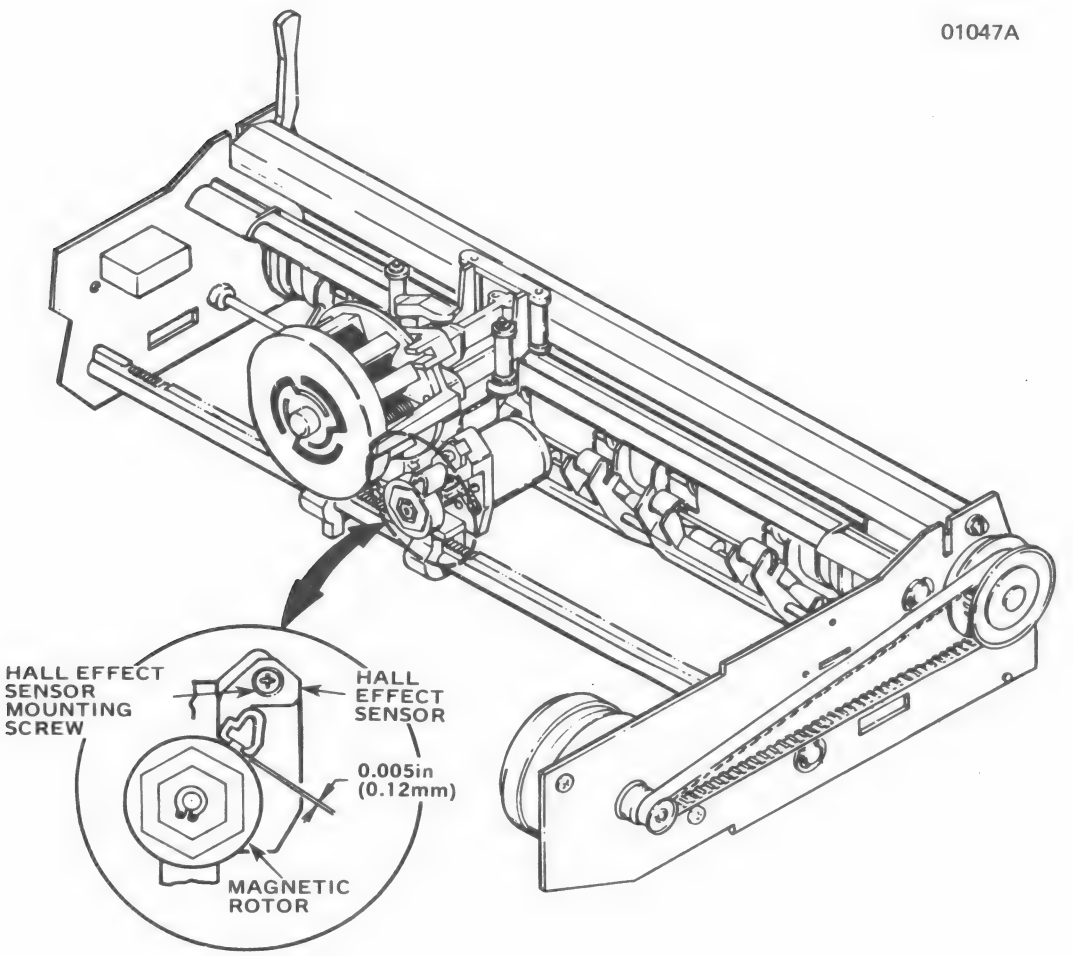


Figure 4-2. HALL EFFECT SENSOR ADJUSTMENT

4.5 PRINT SPEED ADJUSTMENT

1. Remove cover assemblies.

2. Set up printer for self-test per Operators Manual (paragraph 5.5).

3. Place POWER ON/OFF switch in ON position and observe that the power on LED illuminates.

4. Place ON-LINE LOCAL switch in ONLINE position. The print head should move to the left margin, then to the right margin and back. Each time the print head reaches the right margin and reverses direction a line feed is executed. This action continues until the printer is turned off or the ONLINE/LOCAL switch is placed in the LOCAL position.

5. Determine the number of times the print head moves from left to right in one minute (lines per minute) by observing print head movement and using a watch or clock. The proper rate is from 37 to 39 lines per minute.

6. Adjust potentiometer R25 until the proper rate (37 to 39 lines per minute) is achieved.

NOTE

If a scope is available, monitor Column Interrupts at TP1 or U3, pin 6 (see Figure 4-3). Adjust potentiometer R25 for a time interval of 1.0 to 1.1 milliseconds between pulses (with carriage moving forward).

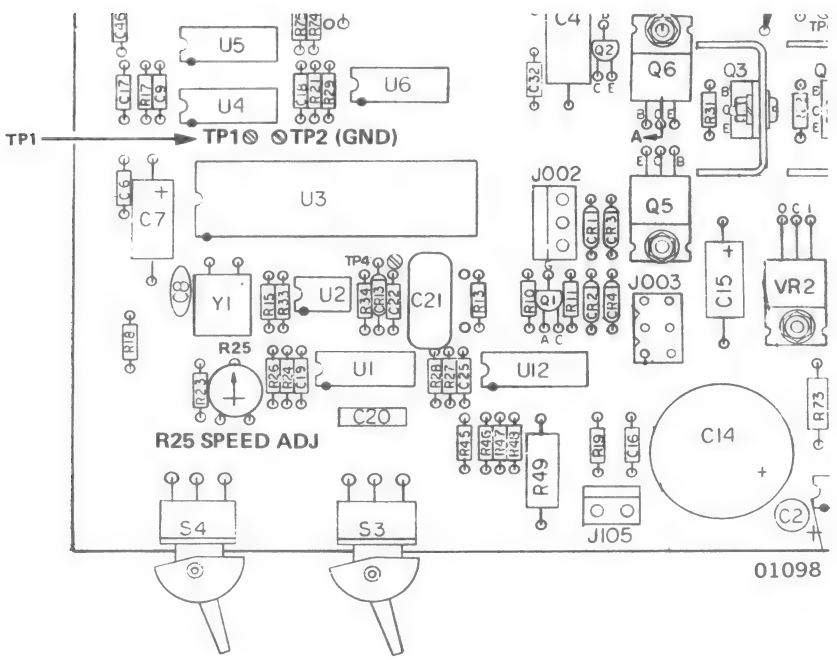


Figure 4-3. PRINT SPEED ADJUSTMENT

4.6 PAPER OUT SWITCH ADJUSTMENT

The Paper Out switch must be adjusted properly; otherwise, either the printer will be disabled, or will run even without paper. If the switch is unplugged, the printer will run without paper.

1. Remove the power connector, the top cover and body cover assembly per the Operators Manual.

2. Remove the mechanism assembly from the printer.

3. Refer to Figure 4-4. Loosen the pivot screw slightly and loosen the locking screw to allow adjustment.

4. Insert a sheet of paper in the normal way so that the actuator arm is depressed.

5. Monitor the microswitch position by attaching an ohmmeter to the two-wire connector. The proper condition of the microswitch is as follows:

   - Paper In; open circuit (infinity on meter).
   - Paper Out; closed circuit (zero ohms, approximately).

6. Turn the Allen (.050") cap screw C.C.W. until the switch closes (zero ohms), then turn C.W. until the switch opens; then 1/4 turn C.W. (to position the actuator arm reliably).

7. Tighten the locking screw and the pivot screw. Check to see that the switch condition of step 5. is reliably met. Repeat step 6. if necessary.

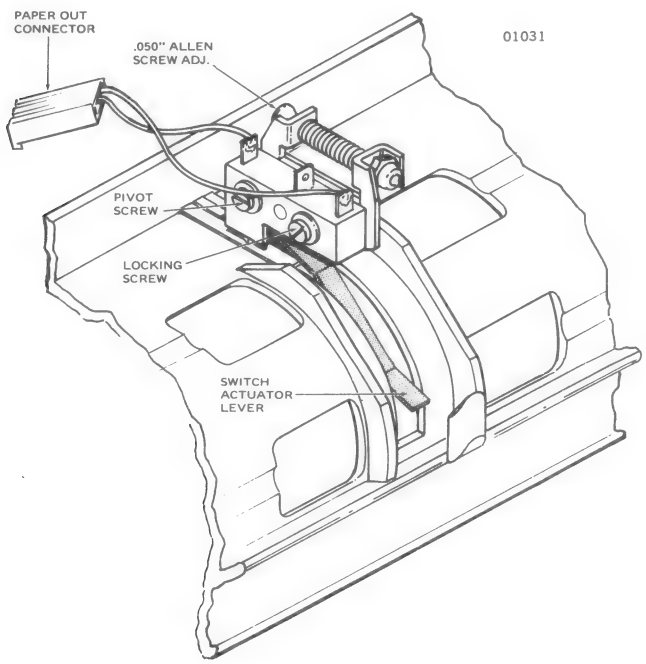


Figure 4-4. PAPER OUT SWITCH ADJUSTMENT

SECTION 5

REMOVAL AND REPLACEMENT

5.1 SCOPE OF THIS SECTION

This section contains removal and replacement procedures which should be performed by trained service personnel. Some procedures require adjustments. Replacement of the fuses is contained in the Operators Manual.

WARNING

Remove plug from the wall outlet before performing any procedure in this section.

5.2 SPARE PARTS

Table 5-1 is a list of spare parts for the Model 739 printer. Parts should be ordered from Centronics Data Computer Corporation, Hudson, New Hampshire 03051. This list of spare parts is for service locations where only major subassemblies are replaced. This section contains procedures for their replacement.

Table 5-1. Spare Parts

Logic PCB (120V, 60 Hz)	63680192-4001	739-1, 739-3, 739-5
Logic PCB (230V, 50 Hz)	63680192-4002	739-2
Logic PCB (230V, VDE)	63680192-4101	739-2L, 739-4L, 739-6L
Mech. Assy. (short)	63680202-5007	739-1, 739-2, 739-3, 739-5
Mech. Assy. (long, VDE)	63680202-5006	739-2L, 739-4L, 739-6L
FF Head Assy.	62001211-5002	All non-VDE units
FF Head Assy. (VDE)	62001211-5003	VDE units
739 Serial I/F PCB; RS232C (512)	63680183-4101	739-3, 739-4
739 Serial I/F PCB; RS232C (2K)	63680183-4102	739-3B, 739-4B

5.3 COVER ASSEMBLY REMOVAL PROCEDURE

The cover assemblies are removed before replacing fuses (non-VDE units), logic PCB or mechanism assembly.

1. Remove power plug from power outlet.

2. Remove top cover by lifting upward at the rear.

3. Remove two Phillips screws from deep holes near front of printer and three Phillips screws from shallow holes at rear of body cover.

4. Unplug ribbon static grounding connector from right side of mechanism assembly.

5. Lift body cover upward, unthread ribbon from printhead and unplug ribbon motor connector J002.

6. Remove slack from ribbon by turning ribbon drive knob clockwise. Place body cover aside.

NOTE

When reassembling body cover onto printer, make connections in this order: J002 ribbon connector, ribbon static ground connector.

5.4 MECHANISM ASSEMBLY REMOVAL/REPLACEMENT

- REMOVAL -

1. Remove cover assemblies per paragraph 5.3 (observe safety Warning).

2. Refer to Figure 5-1. Move print head to left to allow access to ground connectors. Handle print head by sturdy casting area near hex bolts.

3. Unplug stepper motor connector J003 (see Caution).

CAUTION

When unplugging J003, lift by connector body only. Do not pull on wires.

4. Disconnect green ground wire (E4) from lug on right side of mechanism assembly.

5. For VDE units, disconnect power line ground wire (green-yellow) from lug on right side of mechanism assembly.

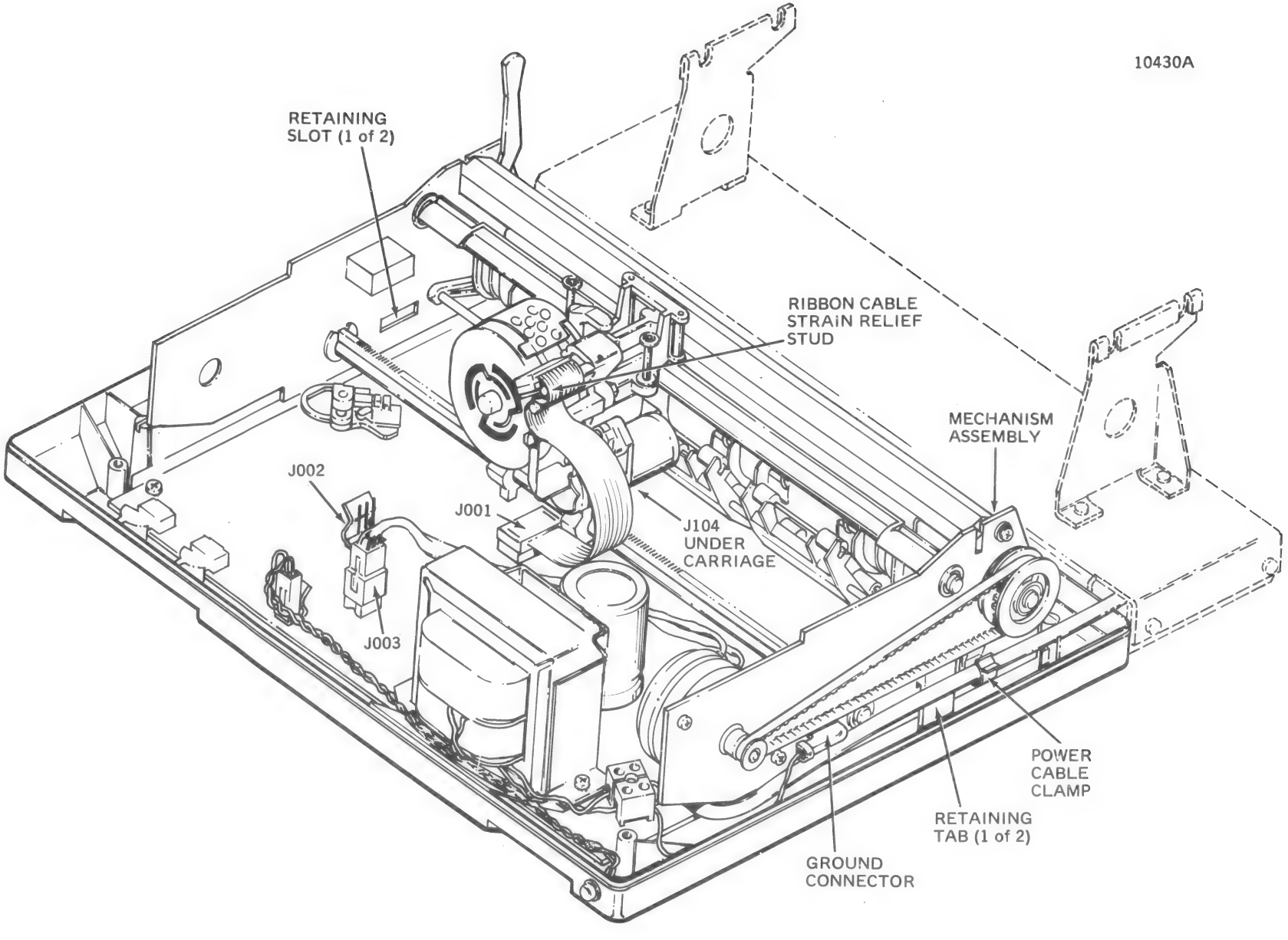


Figure 5-1. MECHANISM ASSEMBLY REPLACEMENT

6. Move print head over to right margin position.

7. Unplug J104 Paper Out switch connector.

8. Carefully unplug J002 ribbon cable connector (see Caution).

CAUTION

Take care not to bend pins on plug when unplugging. Also, pins are sharp and could cause minor injury to fingers. The connector can safely be removed by sliding a long, thin, flat-blade screwdriver between plug and socket (lengthwise) while pressing down on top of plug to prevent excessive tilting.

9. Remove mechanism assembly from base by unlatching the left retaining tab, then the right. Unsnap the nylon power cord clamp on right side of mechanism assembly plate.

- REPLACEMENT -

1. Prepare new mechanism assembly by performing 4.3 Print Head Gap Adjustment, 4.4 Rotor/Hall Effect Sensor Clearance and 4.6 Paper Out Switch Adjustment (only if required).

2. Transfer the flexible cable to the new mechanism assembly (see Caution). Note how ribbon is looped behind head assembly stud for strain relief.

CAUTION

Use thin, flat-blade screwdriver (as described in step 8) to remove plug on flex circuit. Do not pull up on plug, as damage to the flex circuit could occur.

3. Before installing new mechanism assembly, move the print head away from the left margin area to insure that carriage assembly is to the right of the RTP switch arm (see Caution).

CAUTION

Do not install mechanism assembly with print head at left margin. If carriage is on left side of RTP switch arm, damage to the rack will occur on power up.

4. Align new mechanism assembly onto base so that end plates index with locator slots provided for proper seating. Latch retaining tabs at each side of mechanism.

CAUTION

Make certain that no wires or plugs are trapped beneath the mechanism assembly.

5. Place the power cord in the nylon cable clamp and close the clamp.

6. With the print head over to the right margin area, connect the following plugs: J104 Paper Out switch connector; J003 stepper motor connector; J002 ribbon cable connector.

7. Move the print head to the left margin area and connect the following: Green ground wire (E4) to outside lug on right side of assembly plate; for VDE units only, green-yellow power ground wire to bottom lug on inside of right side plate. Note that the top lug is for the ribbon static ground wire, which is on the body cover assembly.

8. Reassemble the body cover assembly, connecting the ribbon static ground wire and J002 ribbon motor connector. Insert and tighten 5 screws. Thread the ribbon around the guide posts and in front of the print head as described in the Operators Manual.

5.5 HEAD-CARRIAGE ASSEMBLY REPLACEMENT (Reference Figure 5-2)

Replacement of the head-carriage assembly requires removal of the assemblies as follows:

1. Place the power switch in the OFF position and remove plug from the wall outlet. Remove the cover assemblies per paragraph 5.3.

2. Remove the mechanism assembly per paragraph 5.4.

> CAUTION
> When removing the carriage shafts in the following steps, take care not to score the shafts, as this could result in rough carriage movement or excessive wear of the carriage. Also, the carriage must be supported and handled carefully during removal and replacement.

3. Remove the two outside retaining rings from the carriage shafts at the right side plate, using a 1/4" flat blade screwdriver, then remove the four inside retaining rings from the carriage shafts. Note orientation of retaining rings (upward "U") for replacement.

4. Remove the rack tension leaf spring from the left side plate using a 6.5 mm (1/4") nut driver. Note orientation of leaf spring for replacement.

5. Carefully press the right ends of the carriage shafts through the side plate, and move them out through the left side plate.

6. Remove the molded rack from the mechanism assembly and set the defective head-carriage assembly aside.

7. Align the replacement head-carriage assembly and insert the nylon rack through the carriage bushings, then index the ends of the rack into the slots in the side plates. See CAUTION below.

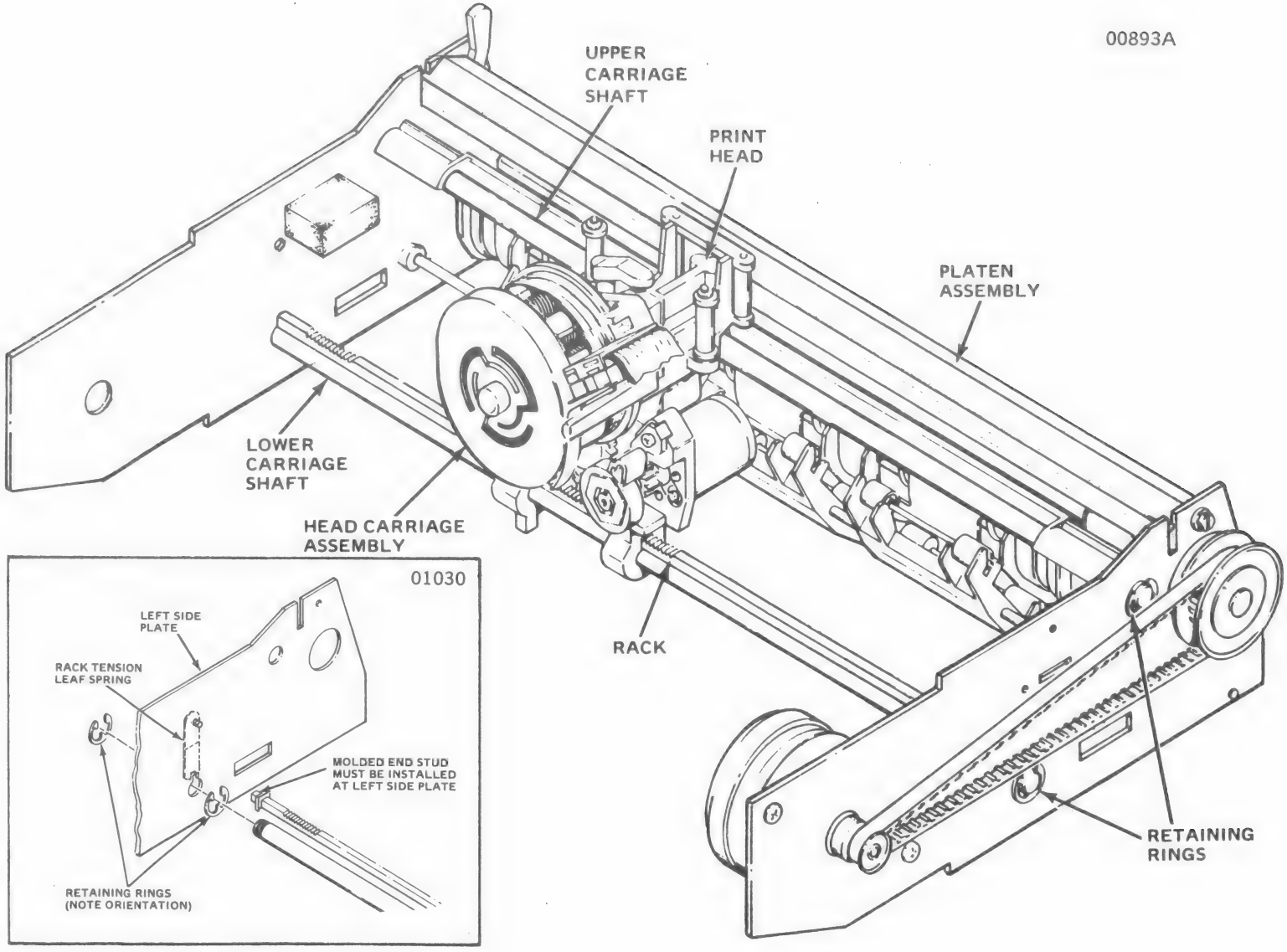


Figure 5-2. HEAD-CARRIAGE ASSEMBLY REPLACEMENT

CAUTION

The rack is not symmetrical, and must be installed so that the end with the molded stud is at the left side plate. The additional rack teeth on the left end are required for the RTP function.

8. Install the carriage shafts and rack tension leaf spring, referring to steps 5., 4., and 3. (reverse order) as required. See NOTE below.

NOTE

Before installing the mechanism assembly on the base, perform 4.3 Printer Head Gap Adjustment, 4.4 Rotor/Hall Effect Sensor Clearance and 4.6 Paper Out Switch Adjustment.

9. Install the mechanism assembly and cover assemblies, referring to steps 2. and 1. (reverse order) as required.

5.6 LOGIC PCB REPLACEMENT

When replacing the logic PCB, removal of the assemblies is required as follows:

1. Place power switch in the OFF position and remove power plug. Remove the cover assemblies per paragraph 5.3.

2. Remove the mechanism assembly per paragraph 5.4. Be certain to read the CAUTIONS for removal/replacement of the mechanism assembly.

3. VDE Units Only - Refer to Figure 5-3. Loosen the two screws on the power terminal block and pull out the blue and brown wires. The nylon cable clamp must be carefully cut to remove the power cable from the PCB. Unplug LED connector J105.

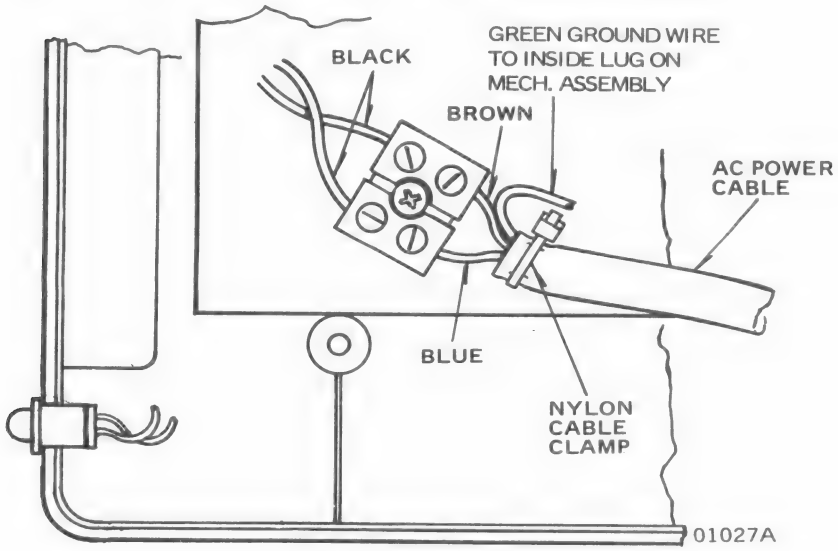


Figure 5-3. POWER CABLE REMOVAL (VDE ONLY)

4. Refer to Figure 5-4 - Remove one Phillips-head screw at the left front corner of the Logic PCB and two Phillips-head screws at transformer T1. Save the transformer heat shields for replacement.

5. Extended Base Units Only - Remove Extended Base cover (4 screws) and carefully unplug ribbon connector from logic PCB. First unplug the ribbon connector from the Serial Interface PCB, then unplug the logic PCB. On the 739-2L, there is no interface PCB; just unplug the ribbon connector from the logic PCB.

CAUTION

When removing the PCB from the base, or when inserting the replacement PCB, take care not to damage the switches, which extend out of the front panel.

6. Disengage the rear edge of the PCB from the rear slots by sliding it toward the front. Lift up at the rear edge and carefully pull the PCB out of the base.

7. Install the replacement PCB, making certain that the shields from step 4. are properly installed, and that the line cord strain relief is replaced on the PCB as shown in Figure 5-3 (VDE units). Refer to steps 6. through 1. (reverse order).

8. VDE Units Only - Dress the LED wire past the front of transformer T1 and plug in J105.

5.7 SERIAL I/F PCB REPLACEMENT

1. Remove the power plug from power outlet.

2. Refer to Figure 5-5. Remove the Serial Interface cover (4 screws).

3. Unplug the ribbon connector from the Serial PCB by carefully prying upward on the tab at each end of the connector alternately, using a screwdriver.

4. Unplug the ribbon connector from the rear edge of the Logic PCB (remove body cover if additional clearance is required).

5. Remove two mounting screws (plus washers and nuts) from the input connector.

6. Remove three PCB mounting screws (plus washers) from the Serial PCB.

7. Carefully remove the Serial PCB from the Serial Interface compartment.

8. Set Switchpack #1 and #2 (SW1, SW2) on replacement PCB according to Operators Manual Interface Information. This is mandatory.

9. Carefully install replacement PCB in reverse order to above. It may be easier to plug the ribbon connector into the Logic PCB first, before mounting the Serial PCB.

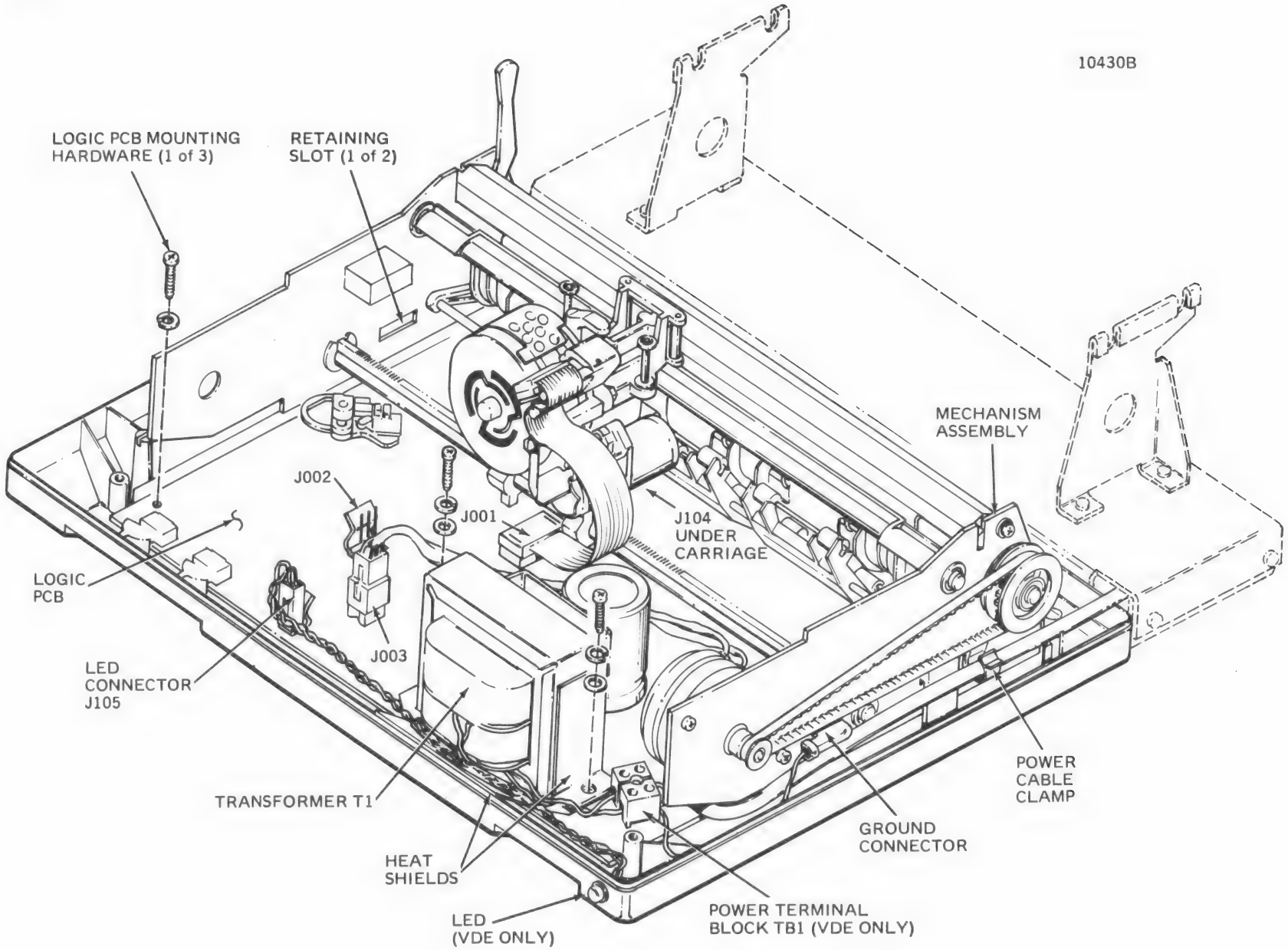


Figure 5-4. LOGIC PCB REPLACEMENT

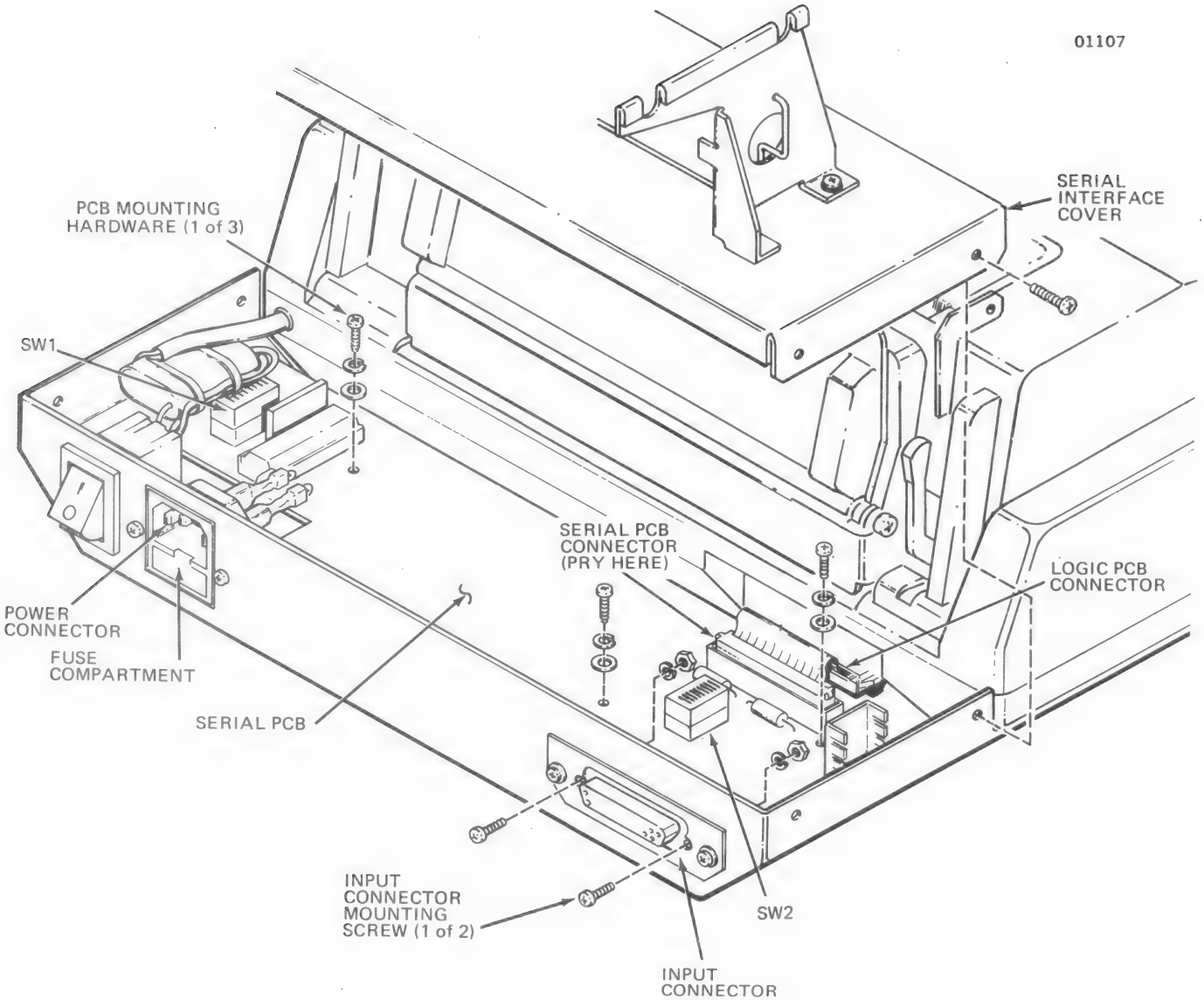


Figure 5-5. SERIAL I/F PCB REPLACEMENT (VDE UNIT SHOWN)

SECTION 6

SUPPORTING ILLUSTRATIONS

6.1 PURPOSE OF THIS SECTION

This section contains drawings and schematics to aid in maintaining and troubleshooting the 739-1 through 739-6 printers.

6.2 MAIN LOGIC BOARD SCHEMATIC (63680193)

The schematic for the main logic PCB is contained in Figures 6-1A, B, C. Inset on Figure 6-1A shows 230V power input circuit for VDE units (739-2L, 739-4, 739-6).

6.3 MAIN LOGIC BOARD ASSY. (63680192)

The assembly drawings for the standard logic PCB and the VDE logic PCB are shown in Figure 6-2 and 6-3.

6.4 SERIAL INTERFACE PCB SCHEMATIC (63680185)

The schematic for the serial interface PCB is contained in Figures 6-4A, B, C, D, E. Note that Figure 6-4C is for 2K buffer and Figure 6-4D is for 512 byte buffer.

6.5 SERIAL INTERFACE PCB ASSY. (63680183)

The assembly drawing for the serial interface PCB is shown in Figure 6-5. The jumper configuration for XON-XOFF is included.

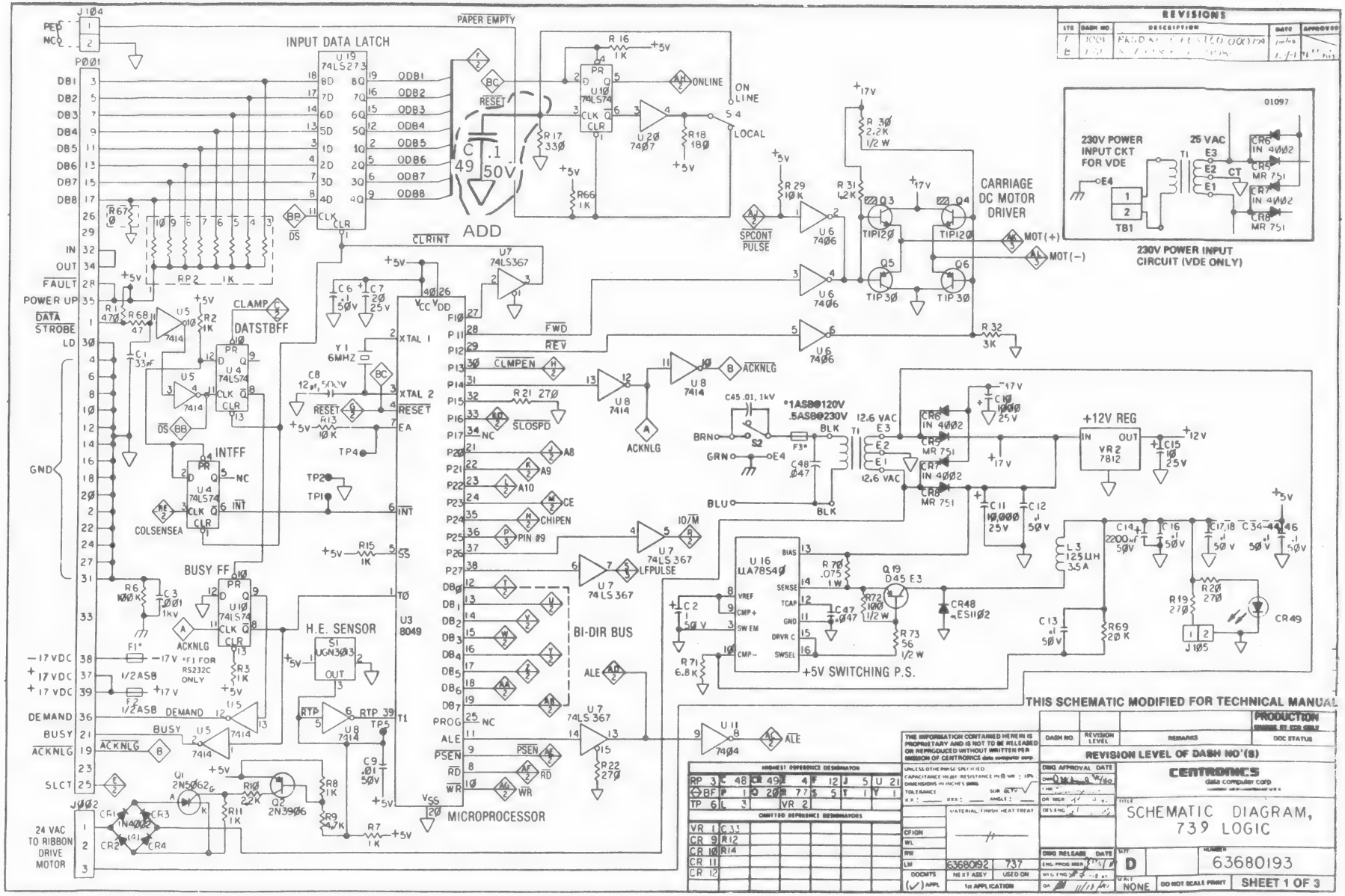


Figure 6-1A. MAIN LOGIC SCHEMATIC (SH1)

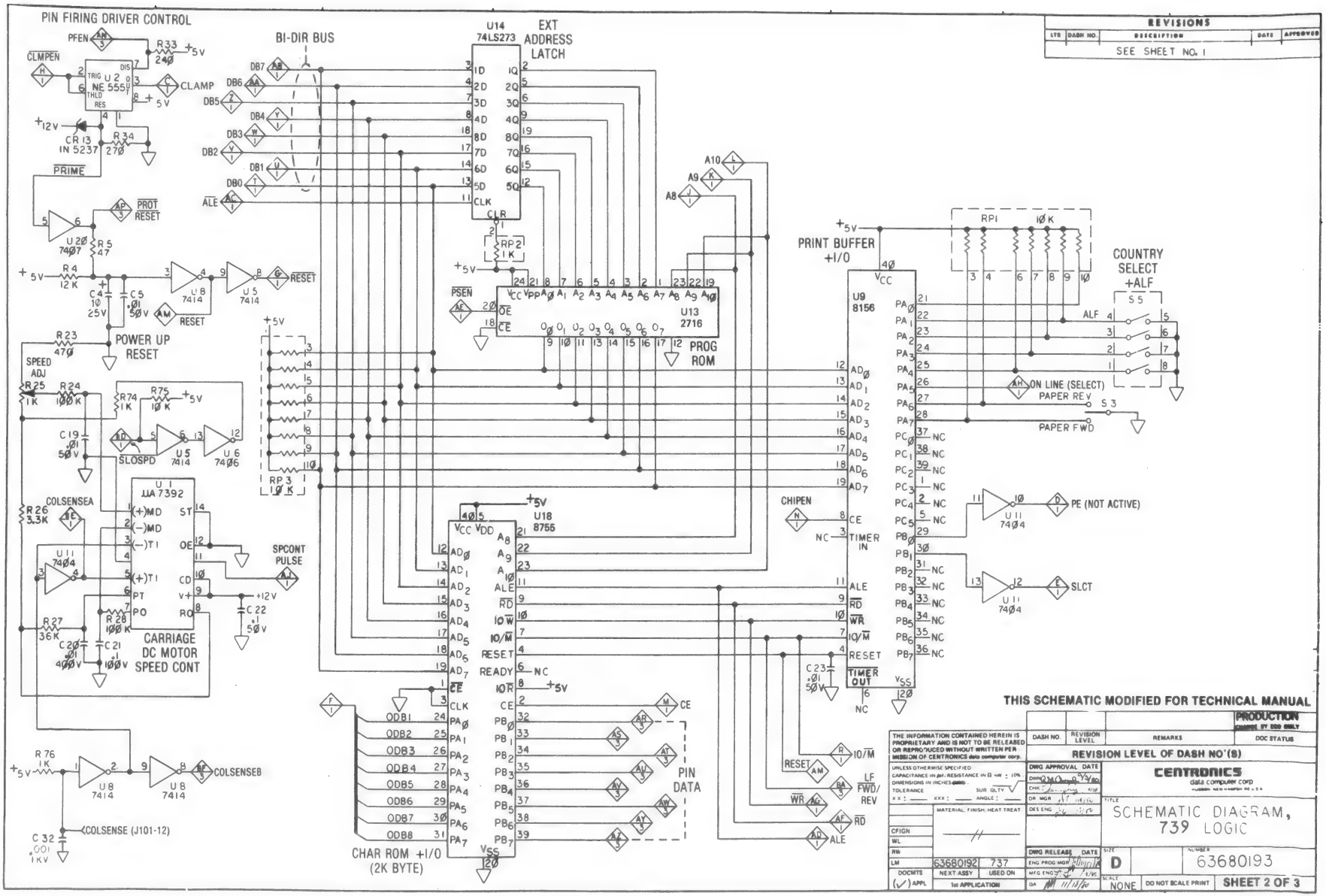


Figure 6-1B. MAIN LOGIC SCHEMATIC (SH2)

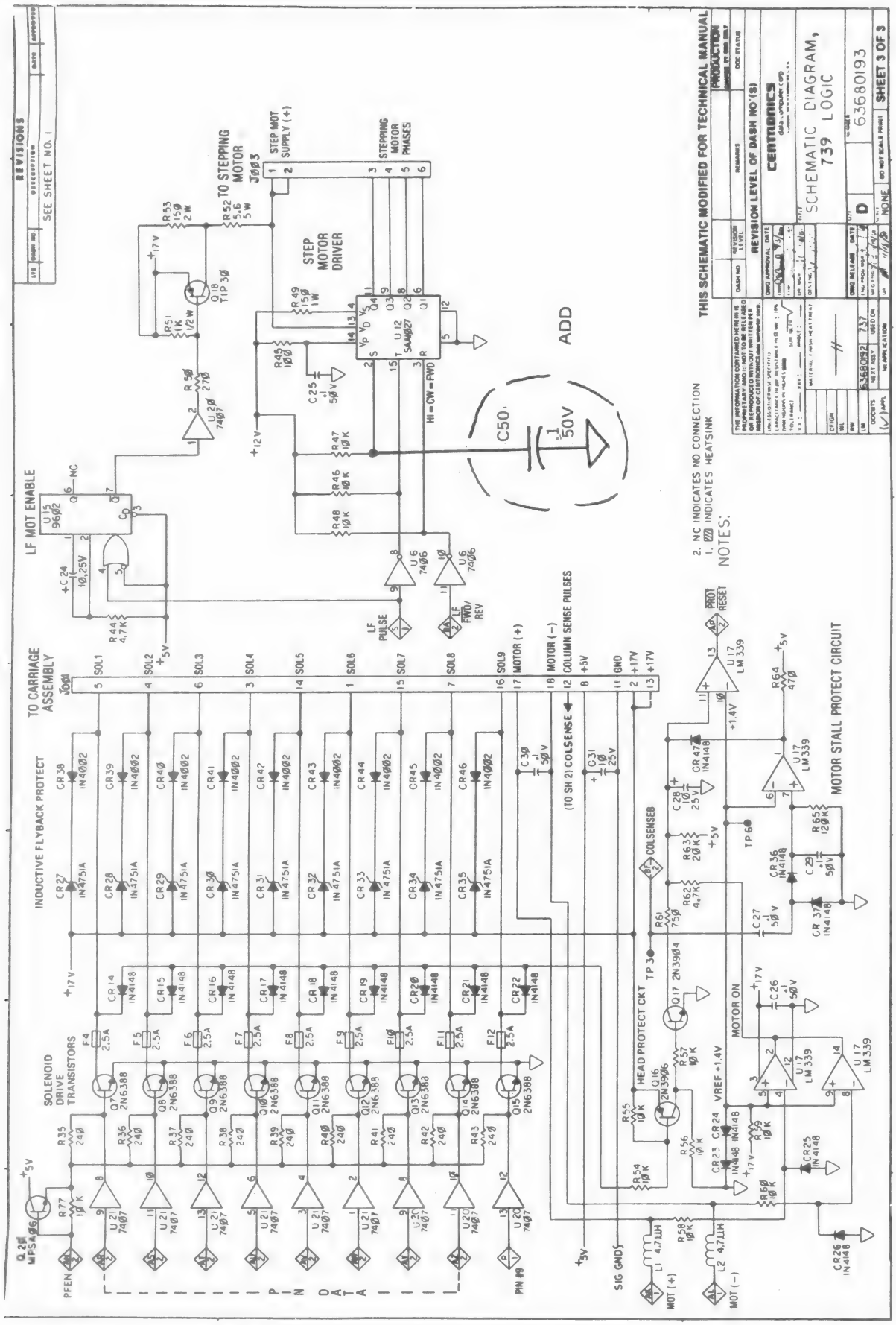


Figure 6-1C. MAIN LOGIC SCHEMATIC (SH3)

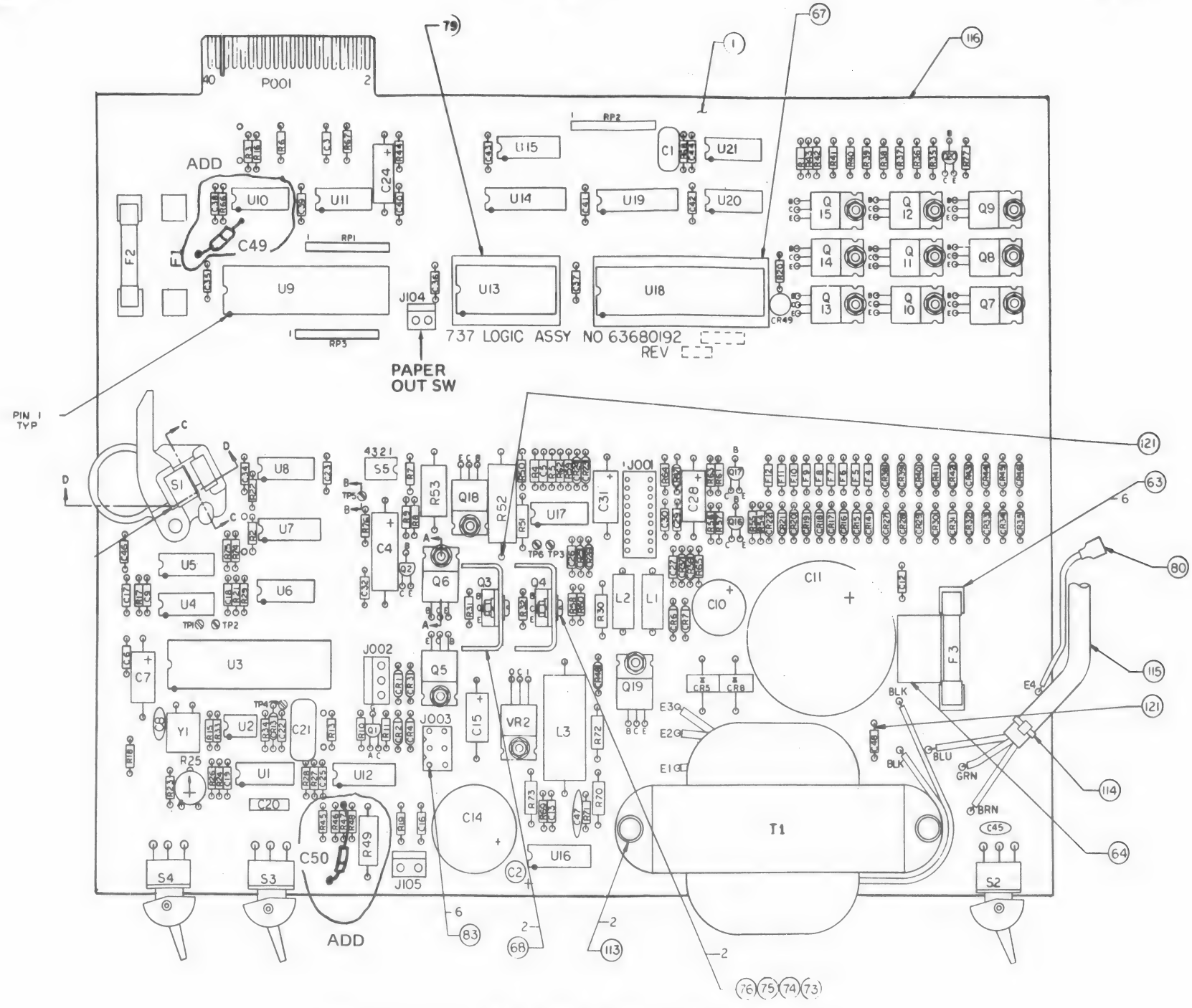


Figure 6-2. MAIN LOGIC ASSY. (NON-VDE UNITS)

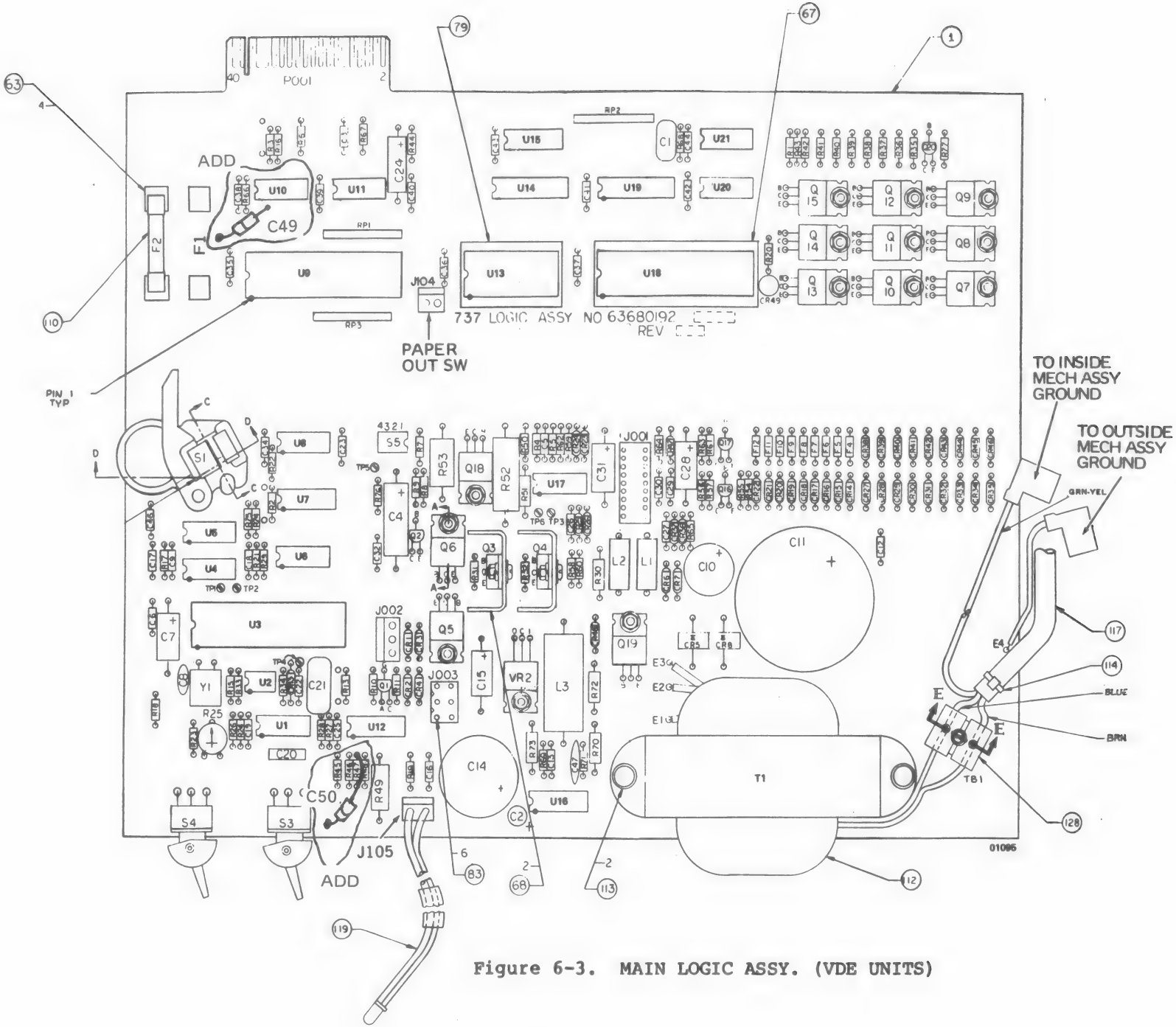


Figure 6-3. MAIN LOGIC ASSY. (VDE UNITS)

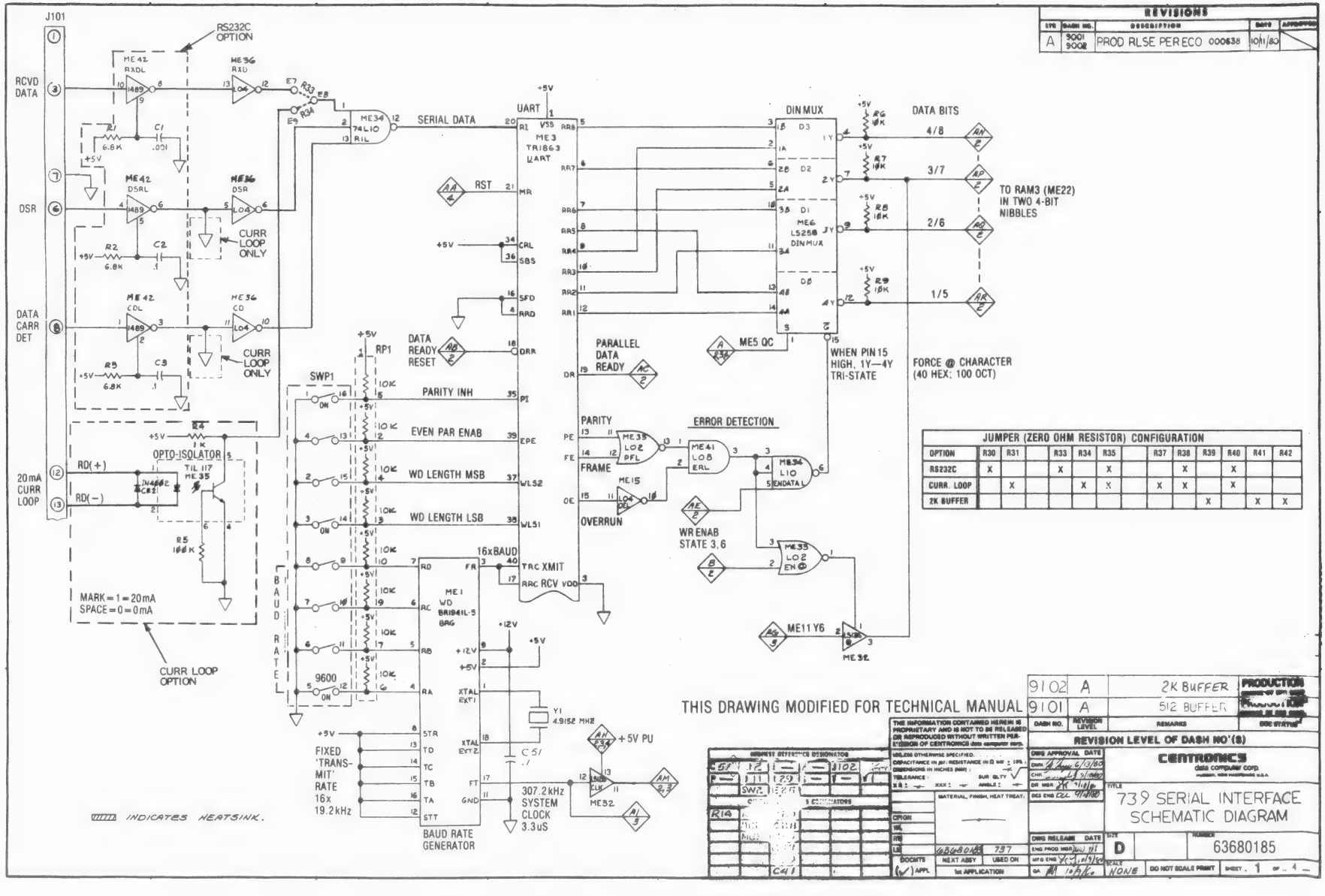


Figure 6-4A. SERIAL INTERFACE SCHEMATIC (SH1)

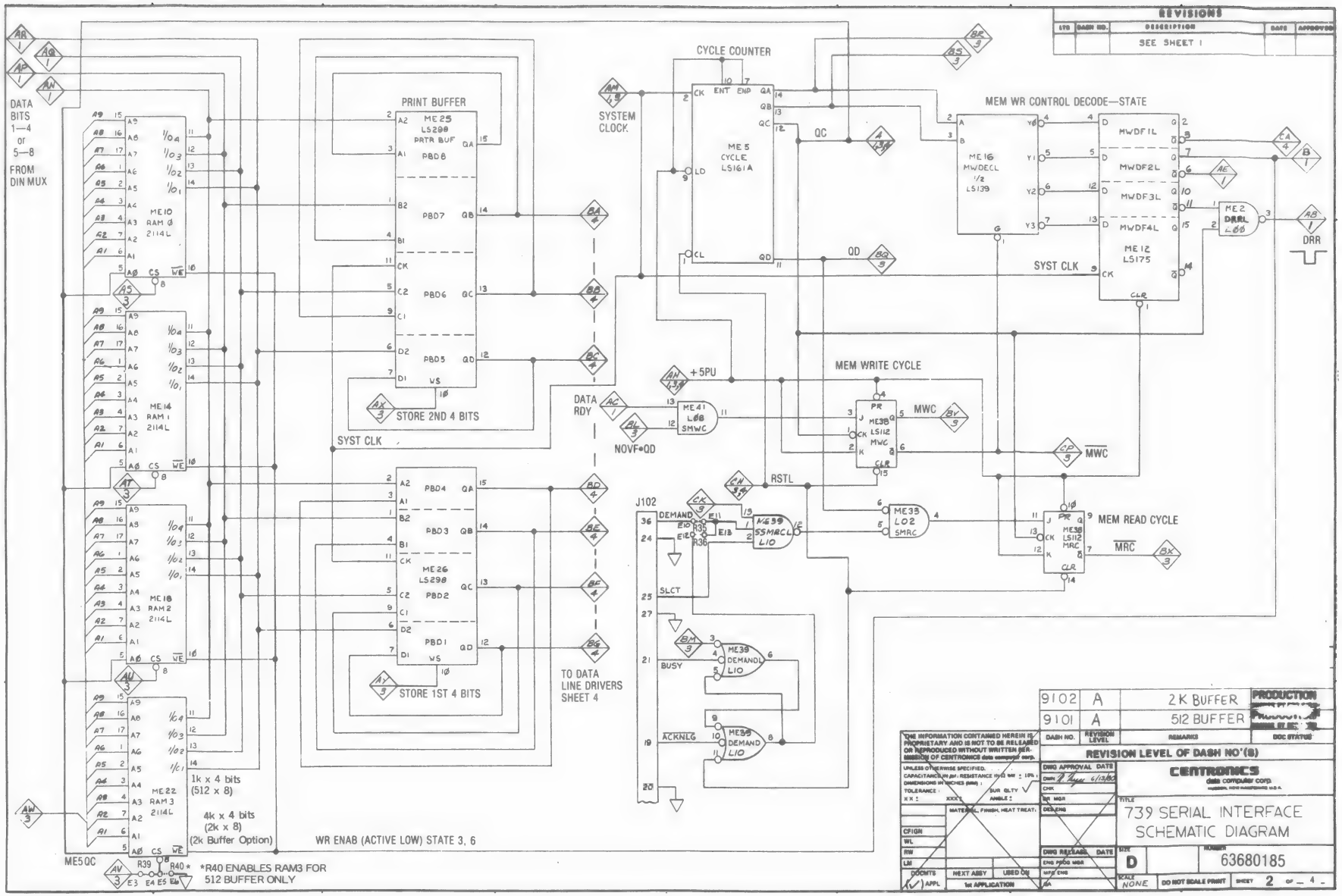


Figure 6-4B. SERIAL INTERFACE SCHEMATIC (SH2)

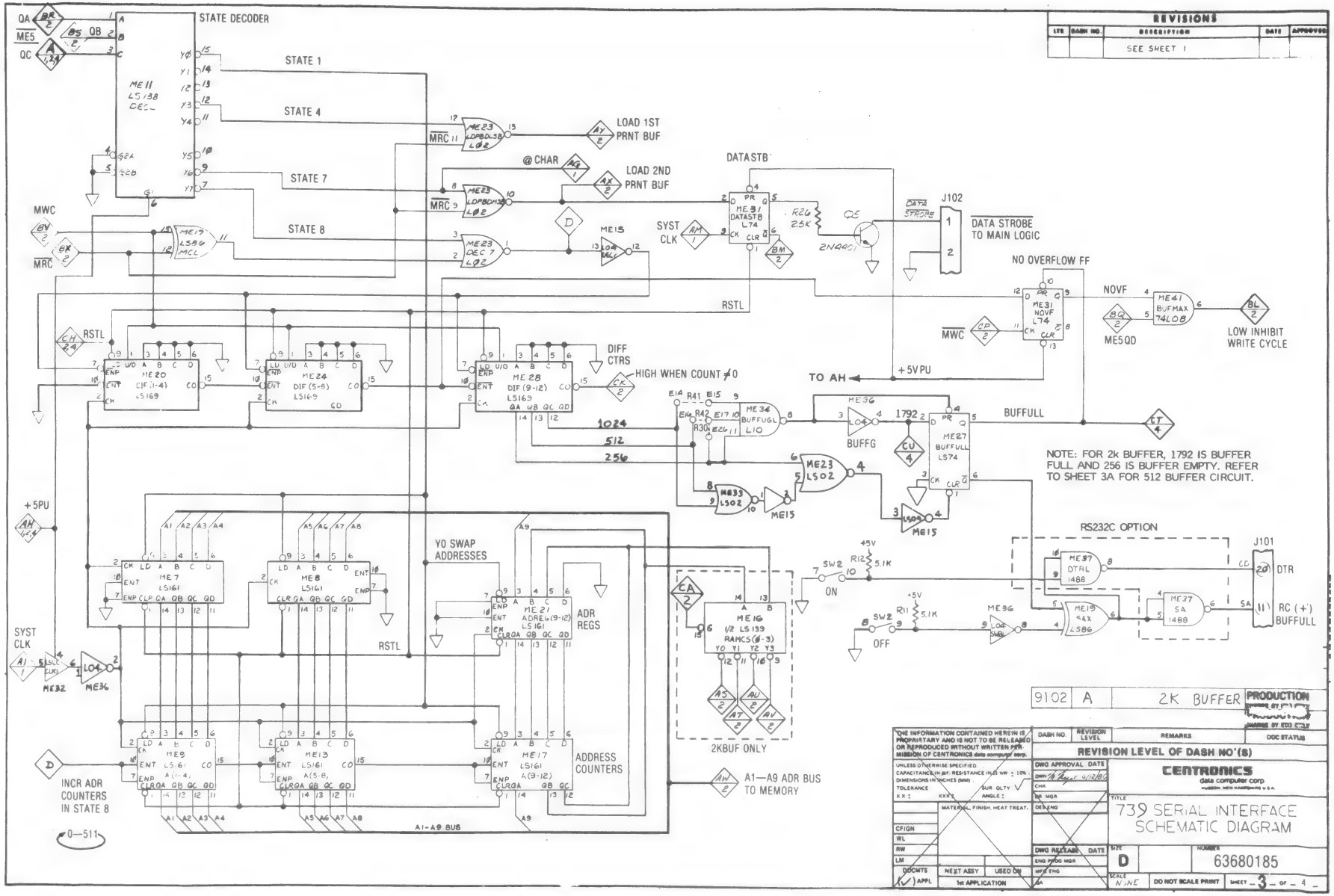


Figure 6-4C. SERIAL INTERFACE SCHEMATIC (SH3)

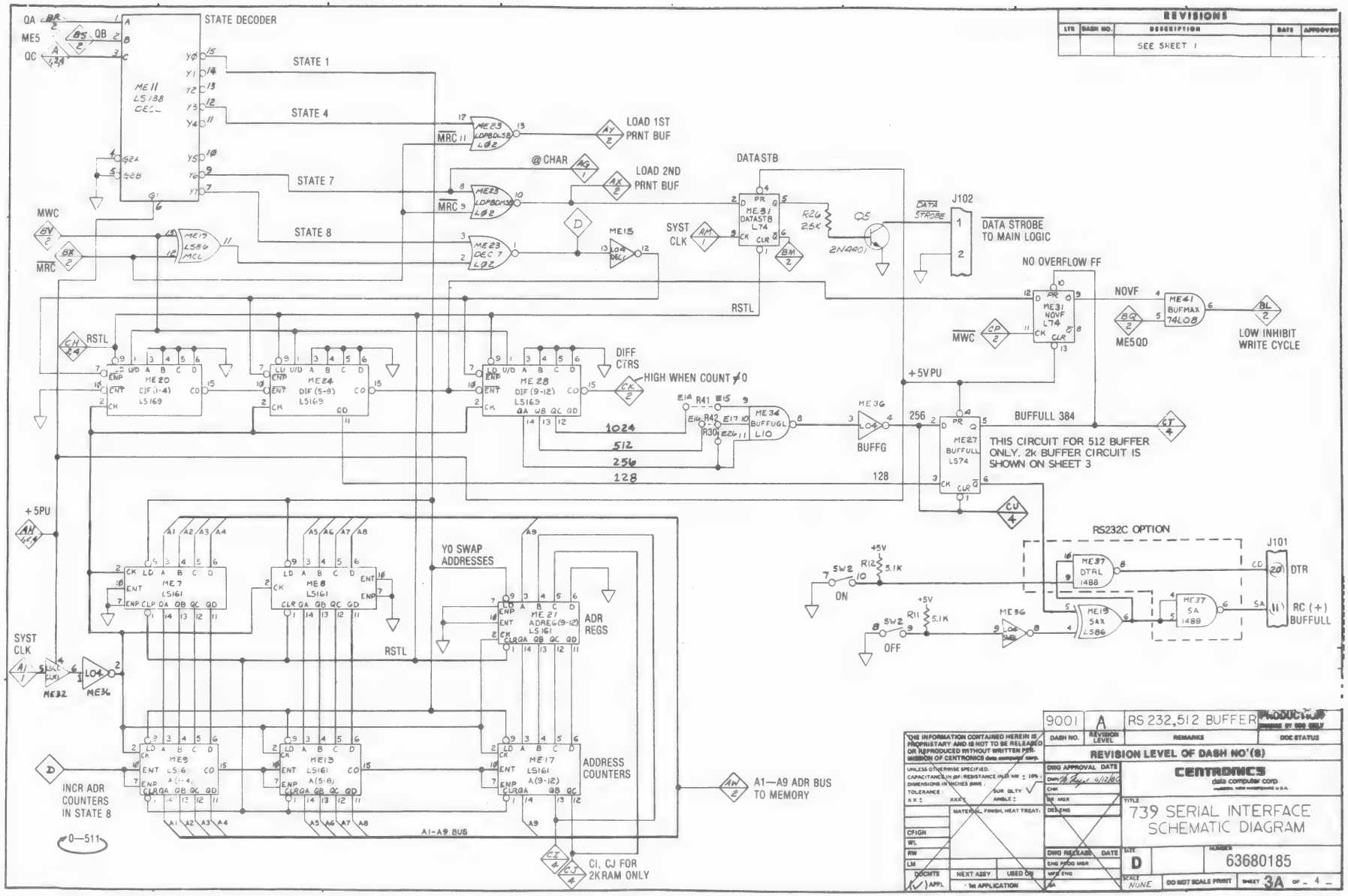


Figure 6-4D. SERIAL INTERFACE SCHEMATIC (SH3A)

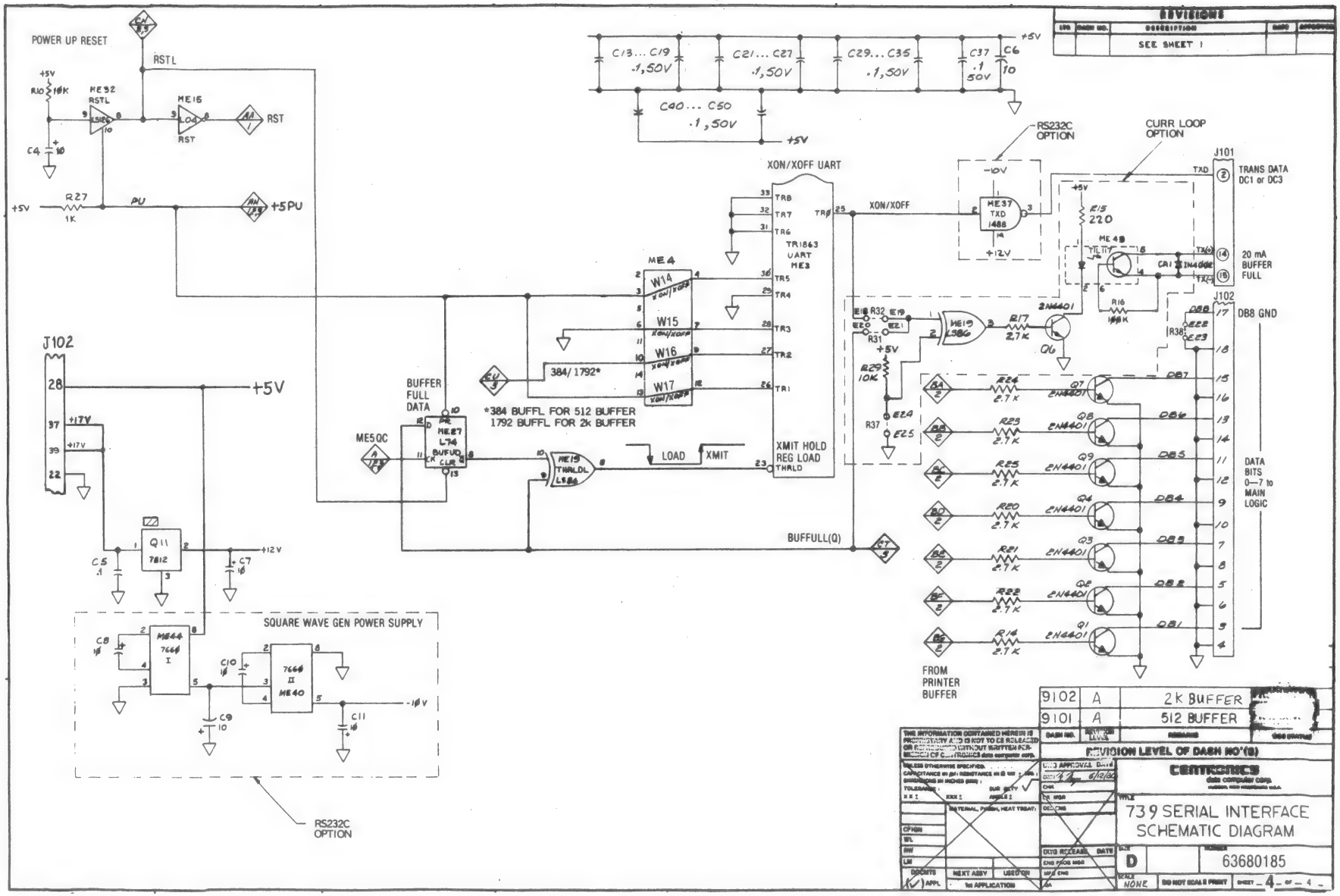


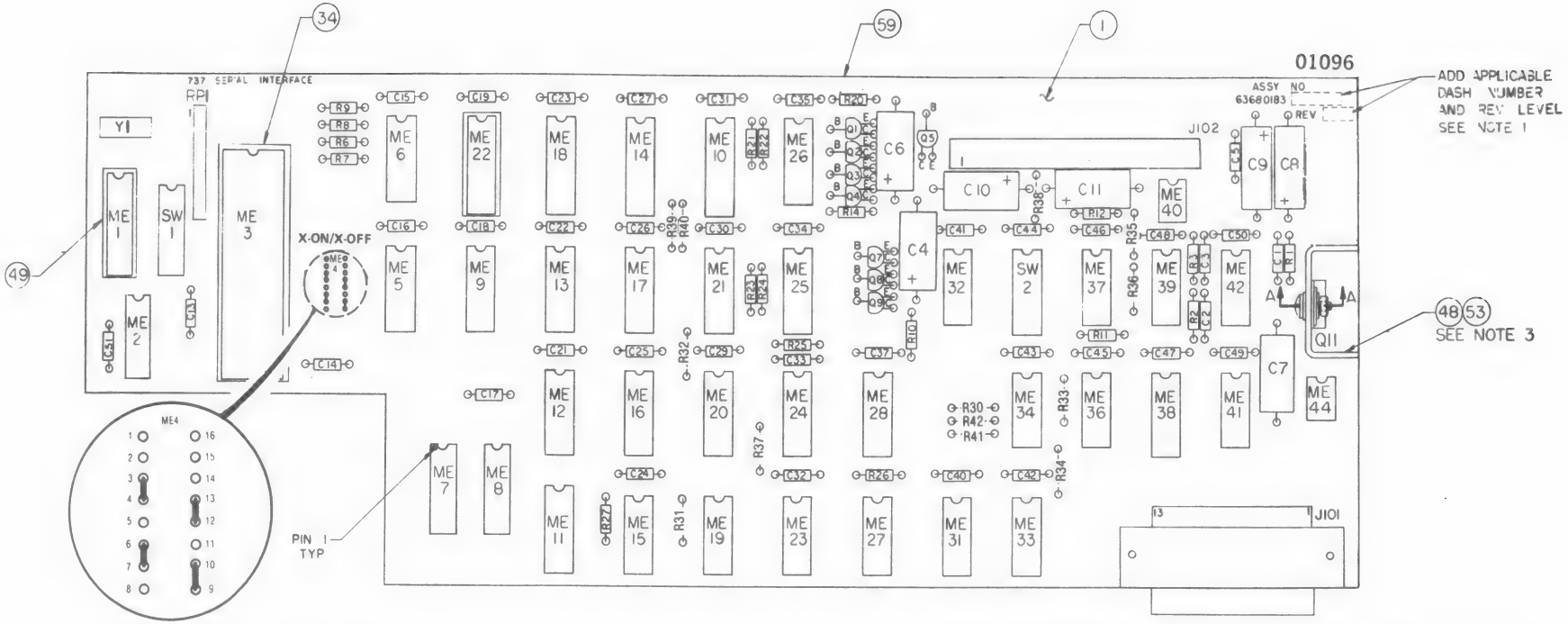
Figure 6-4E. SERIAL INTERFACE SCHEMATIC (SH4)

PART NUMBER CONFIGURATION
63680183-4XXX XXXX XXX

BASIC CONFIGURATION
SEE LIST OF MATERIALS

NOT USED

NOT USED

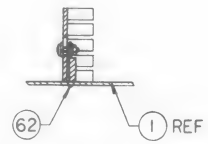


3 APPLY ITEM 53 (SILICON COMPOUND) TO TRANSISTOR MOUNTING SURFACE OF ITEM 48.
2 DOCUMENTS INDICATED (✓) IN TITLE BLOCK ARE LOCATED WITH LM.
1 MARK .12 MIN CHARACTERS AND LOCATE APPROXIMATELY AS SHOWN.

NOTES

THIS DRAWING MODIFIED FOR TECHNICAL MANUAL

NOTE: SOME COMPONENTS SHOWN ON DRAWING MAY NOT BE ON PCB DEPENDING ON DASH CONFIGURATIONS.



SECTION A-A
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	DES ENG [illegible] 9/10/80		PCB ASSY, 739 SERIAL INTERFACE		
MATERIAL, FINISH, HEAT TREAT: —					
REF DES ✓					
CFIGN					
WL					
RW ✓					
LM ✓ 4000	DWG RELEASE DATE		SIZE D	NUMBER 63680183	
DOCMTS (✓) APPL NEXT ASSY 737 USED ON 1st APPLICATION	ENG PROG MGR [illegible] 9/11				
	MFG ENG [illegible] 10/1/80				
	QA [illegible] 10/1/80		SCALE 2/1	DO NOT SCALE PRINT	SHEET — OF —

Figure 6-5. SERIAL I/F PCB ASSEMBLY

READERS COMMENTS

Publications Title Model 739 Printer Technical Manual

Publications No. 37400910-9001 Revision B Date February 1982

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